

# Product Document



**AS3722– OTP Specification -09**

**AS3722-BCTT-09**

**AS3722-BWLT-09**

**OTP Specification -09**

## Table of Contents

1	General Description .....	3
2	OTP Description .....	3
2.1	GUI SW screenshot .....	3
2.2	Start-up file .....	5

## Revision History

Revision	Date	Owner	Description
0.90	25.10.2013	pkm	Initial version
1.0	26.11.2013	pkm	Updated NVPN
1.09	17.01.2014	pkm	Updates for chip version 1v21
1.10	23.01.2014	pkm	Updated NVPN
1.20	28.3.2014	pkm	added MPN

## 1 General Description

The “-09” OTP version is applicable for the following ordering codes:

Ordering code	MPN	Reel Size	NVPN
AS3722-BCTT-09	193600016	500pcs	315-0268-000

The silicon version used for these build used 1v21.

## 2 OTP Description

File name: AS3722\_OTP-09\_nVidia\_1V35mem\_3S\_-200mV\_20131025.txt

### 2.1 GUI SW screenshot

**General Settings**

UID Reset Slots

Delay Interval: 4 ms

Reset time: 11ms ncells:

Reset Voltage Rise: 8.85V 3 cell: reset\_rise = 3\*(2.5...3.6) = 7.5...10.8

vsup\_min: 4.5V

SupResEn  auto off

em\_shutdown\_direct  pwr\_off vsuplow

rtc\_on  wtdg\_on Watchdog mode: INT only

ENABLE2\_invert  ENABLE3\_invert  GPIO12 pulldown

LID\_pwr\_on  LID invert  GPIO12 input

ac\_ok\_pwr\_on  ac\_ok\_invert  therm\_invert

onkey\_lpress\_res  onkey\_invert  I2C pullup

Onkey Shutdown Delay: 8sec

SD2 fast  SD2 hi\_curr  SD0 -200mV offset

SD3 fast  SD3 slave

SD4 fast  SD4 slave multiphase clock: 1.35 MHz

SD5 fast  SD5 slave LDO3 offset: no offset

sd0\_vmax: Protection disabled sd0\_trim\_gr: fast

sd6\_vmax: Protection disabled sd1\_trim\_gr: fast

sd6\_trim\_gr: fast

<b>Timeslot 0</b>	
LDO3	1.1000V
<input checked="" type="checkbox"/> Delayed	Mode PMOS LDO tracking
<b>Timeslot 1</b>	
SD1	1.1000V
<input checked="" type="checkbox"/> Delayed	<input checked="" type="radio"/> Normal <input type="radio"/> Low Power
<b>Timeslot 2</b>	
Not Used	
<input checked="" type="checkbox"/> Delayed	
<b>Timeslot 3</b>	
Not Used	
<input checked="" type="checkbox"/> Delayed	
<b>Timeslot 4</b>	
Not Used	
<input checked="" type="checkbox"/> Delayed	
<b>Timeslot 5</b>	
Not Used	
<input checked="" type="checkbox"/> Delayed	
<b>Timeslot 6</b>	
SD5	1.8000V
<input checked="" type="checkbox"/> Delayed	<input checked="" type="radio"/> 3MHz <input type="radio"/> 4MHz
<b>Timeslot 7</b>	
GPIO2	<input checked="" type="checkbox"/> invert
<input type="checkbox"/> Delayed	IO mode Normal IO operation
	Output (Push/pull) VDDL_GPIO

<b>Timeslot 8</b>	
SD2 <input type="checkbox"/> Delayed	1.3500V <input checked="" type="radio"/> 3MHz <input type="radio"/> 4MHz
<b>Timeslot 9</b>	
LDO0 <input checked="" type="checkbox"/> Delayed	1.0500V <input type="radio"/> 150mA <input checked="" type="radio"/> 300mA
<b>Timeslot 10</b>	
GPIO1 <input checked="" type="checkbox"/> Delayed	<input checked="" type="checkbox"/> invert ID Normal I/O operation mode Output (Push/pull) VDDL_GPIO
<b>Timeslot 11</b>	
GPIO4 <input type="checkbox"/> Delayed	<input type="checkbox"/> invert ID Normal I/O operation mode Output (Push/pull) VDDL_GPIO
<b>Timeslot 12</b>	
Not Used <input type="checkbox"/> Delayed	
<b>Timeslot 13</b>	
Not Used <input type="checkbox"/> Delayed	
<b>Timeslot 14</b>	
Not Used <input type="checkbox"/> Delayed	
<b>Timeslot 15</b>	
Not Used <input type="checkbox"/> Delayed	
<b>Timeslot 16</b>	
Not Used <input type="checkbox"/> Delayed	

## 2.2 Start-up file

### # Fuse Register Settings

- Register 0xa7 = 0x38 (00111000b)
- Register 0xa8 = 0x4f (01001111b)
- Register 0xa9 = 0xe4 (11100100b)
- Register 0xaa = 0x57 (01010111b)
- Register 0xab = 0x7e (01111110b)
- Register 0xac = 0x41 (01000001b)
- Register 0xad = 0x00 (00000000b)
- Register 0xae = 0x00 (00000000b)

Register 0xaf = 0x12 (00010010b)  
Register 0xb0 = 0xfb (11111011b)  
Register 0xb1 = 0x13 (00010011b)  
Register 0xb2 = 0x59 (01011001b)  
Register 0xb3 = 0x32 (00110010b)  
Register 0xb4 = 0xcc (11001100b)  
Register 0xb5 = 0x00 (00000000b)  
Register 0xb6 = 0x00 (00000000b)  
Register 0xb7 = 0x2f (00101111b)  
Register 0xb8 = 0xcc (11001100b)  
Register 0xb9 = 0x00 (00000000b)  
Register 0xba = 0x00 (00000000b)  
Register 0xbb = 0xa5 (10100101b)  
Register 0xbc = 0x50 (01010000b)  
Register 0xbd = 0x87 (10000111b)  
Register 0xbe = 0x2e (00101110b)  
Register 0xbf = 0x02 (00000010b)  
Register 0xc0 = 0x3c (00111100b)  
Register 0xc1 = 0x8a (10001010b)  
Register 0xc2 = 0xc9 (11001001b)  
Register 0xc3 = 0x87 (10000111b)  
Register 0xc4 = 0x07 (00000111b)  
Register 0xc5 = 0x55 (01010101b)  
Register 0xc6 = 0xcc (11001100b)  
Register 0xc7 = 0x00 (00000000b)  
Register 0xc8 = 0x00 (00000000b)  
Register 0xc9 = 0xcc (11001100b)  
Register 0xca = 0x00 (00000000b)  
Register 0xcb = 0x00 (00000000b)  
Register 0xcc = 0x05 (00010101b)  
Register 0xcd = 0xcc (11001100b)  
Register 0xce = 0x00 (00000000b)  
Register 0xcf = 0x00 (00000000b)