

TMD3725

ALS, Color and Proximity Sensor Module

General Description

The device features advanced proximity measurement, color sense (RGBC+IR), and digital ambient light sensing (ALS). The package has been designed to accommodate a “single hole” aperture approach. The slim module incorporates an IR LED and factory calibrated LED driver. The proximity detection feature provides object detection (e.g. mobile device screen to user’s ear) by photodiode detection of reflected IR energy (sourced by the integrated LED). Detect/release events are interrupt driven, and occur when proximity result crosses upper and/or lower threshold settings. The proximity engine features offset adjustment registers to compensate for unwanted IR energy reflection at the sensor. Proximity results are further improved by automatic ambient light subtraction. The ALS detection feature provides photopic light intensity data. The color photodiodes have UV and IR blocking filters and a dedicated data converters producing 16-bit data. This architecture allows applications to accurately measure ambient light which enables devices to calculate illuminance and color temperature to control display backlight and chromaticity.

[Ordering Information](#) and [Content Guide](#) appear at end of datasheet.

Key Benefits & Features

The benefits and features of TMD3725, ALS, Color and Proximity Sensor Module are listed below:

Figure 1:
Added Value of Using TMD3725

| Benefits | Features |
|--|---|
| <ul style="list-style-type: none"> Single glass aperture solution | <ul style="list-style-type: none"> 1.0mm spacing between proximity IR LED and sensor |
| <ul style="list-style-type: none"> Reduced board space requirements and enables low-profile system design | <ul style="list-style-type: none"> Small footprint and low-profile package (3.65 x 2.00 x 1.00 mm) |
| <ul style="list-style-type: none"> Accurate color temperature and ambient light sensing | <ul style="list-style-type: none"> UV / IR blocking filters 46° Average FOV Photopic ambient light sensing (ALS) Programmable gain and integration time |
| <ul style="list-style-type: none"> Compact integrated optical module | <ul style="list-style-type: none"> Color (RGB), Ambient Light and Proximity Sensing with integrated IR LED |
| <ul style="list-style-type: none"> Reduced power consumption | <ul style="list-style-type: none"> Power management features (active, idle and sleep states) 1.8V power supply with 1.8V I²C bus |

Applications

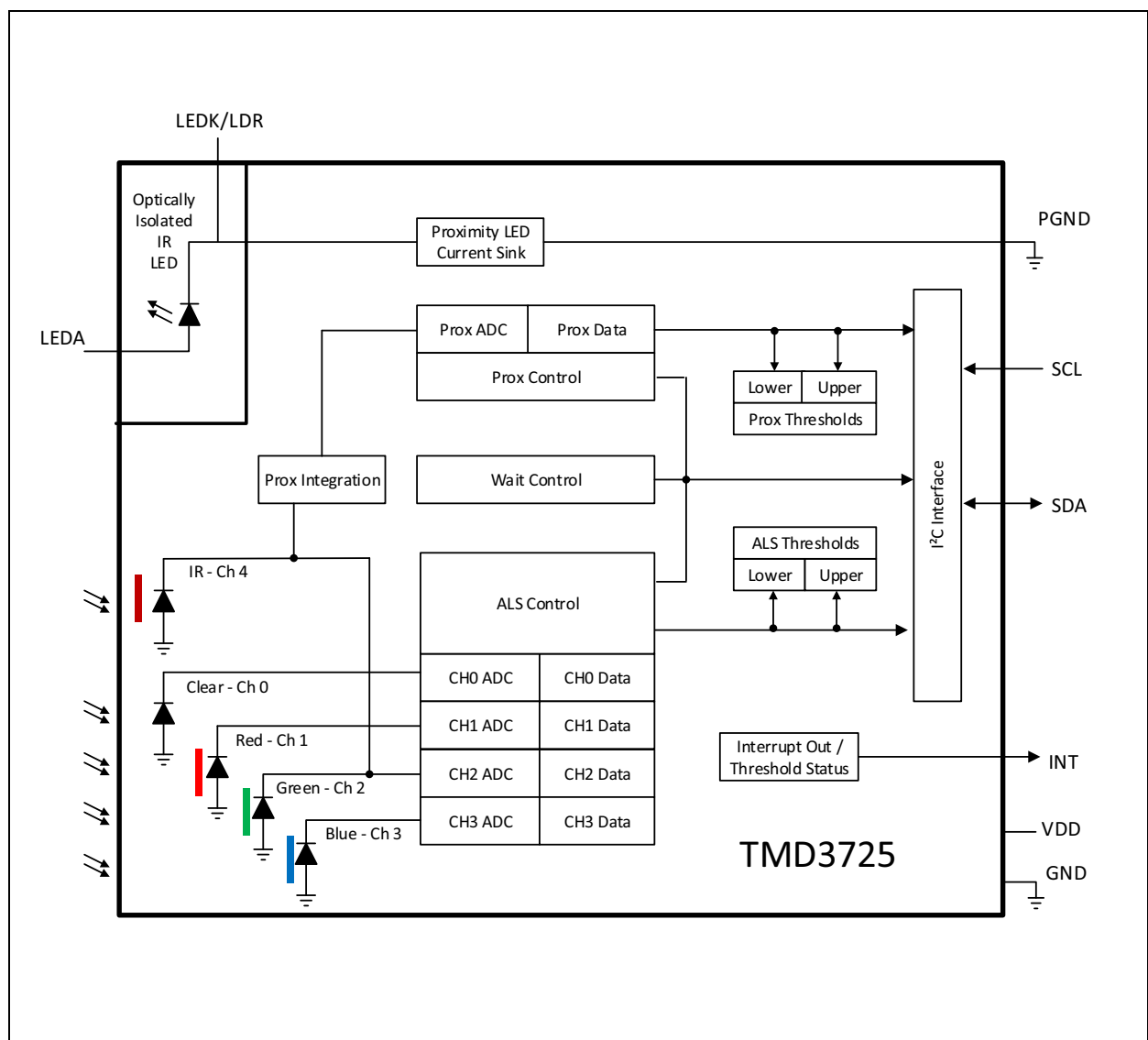
The TMD3725 applications include:

- Ambient light sensing
- Single hole proximity sensing
- Mobile phone touch screen disable
- Color temperature sensing to assist backlight, camera, and flash control

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TMD3725



Pin Assignment

Figure 3:
Pin Diagram of TMD3725

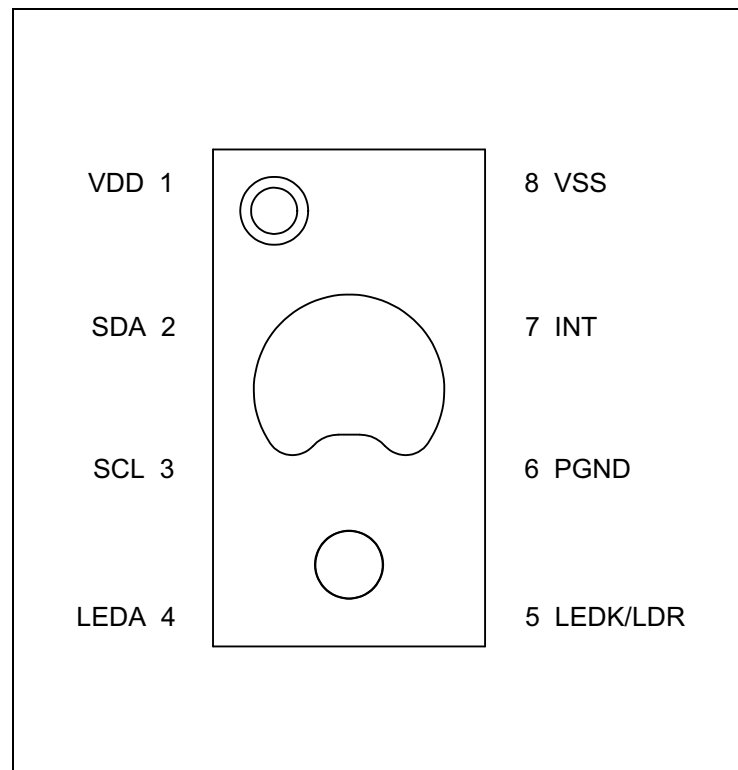


Figure 4:
Pin Description of TMD3725 (8-Pin Module)

| Pin Number | Pin Name | Description |
|------------|----------|---|
| 1 | VDD | Supply voltage |
| 2 | SDA | I ² C serial data I/O terminal |
| 3 | SCL | I ² C serial clock input terminal |
| 4 | LEDA | LED anode |
| 5 | LEDK/LDR | LED driver (sinks current) and LED cathode (for direct access to LED) |
| 6 | PGND | Ground for LED current sink and pins with open drain |
| 7 | INT | Interrupt. Open drain output (active low) |
| 8 | VSS | Ground. All voltages are referenced to GND |

Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | Comments |
|--------------------------------|--|--------|-----|-------|----------|
| Electrical Parameters | | | | | |
| VDD | Supply Voltage to Ground | -0.3 | 2.2 | V | |
| LEDA | LED Voltage to PGND | -0.3 | 3.6 | V | |
| V _{IO} | Digital I/O Terminal Voltage | -0.3 | 3.6 | V | |
| I _{IO} | SDA, INT Output Terminal Current | -1 | 20 | mA | |
| Electrostatic Discharge | | | | | |
| I _{SCR} | Input Current (latch up immunity) JEDEC JESD78D | ±100 | | mA | Class II |
| ESD _{HBM} | Electrostatic Discharge HBM JS-001-2014 | ± 2000 | | V | |
| ESD _{CDM} | Electrostatic Discharge CDM JEDEC JESD22-C101F | ± 500 | | V | |

| Symbol | Parameter | Min | Max | Units | Comments |
|--|------------------------------------|-----|-----|-------|--|
| Temperature Ranges and Storage Conditions | | | | | |
| T_A | Operating Ambient Temperature | -30 | 85 | °C | |
| T_{STRG} | Storage Temperature Range | -40 | 85 | °C | |
| T_{BODY} | Package Body Temperature | | 260 | °C | IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." |
| RH_{NC} | Relative Humidity (non-condensing) | 5 | 85 | % | |
| MSL | Moisture Sensitivity Level | 3 | | | Maximum floor life time 168 hours |

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Operating Characteristics, VDD = 1.8V, T_A = 25°C (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|--|---|------|-----|------|------|
| f _{OSC} | Oscillator frequency | | | 8.0 | | MHz |
| IDD | Supply current ⁽¹⁾ | Active ALS State (PON=AEN=1, PEN=0) ⁽²⁾ | 50 | 90 | 150 | μA |
| | | Idle State (PON=1, AEN=PEN=0) ⁽³⁾ | | 30 | 60 | |
| | | Sleep State ⁽⁴⁾ | | 0.7 | 5.0 | |
| VOL | INT, SDA output low voltage | 6mA sink current | | | 0.6 | V |
| ILEAK | Leakage current, SDA, SCL, INT | | -5 | | 5 | μA |
| VIH | SCL, SDA input high voltage ⁽⁵⁾ | | 1.26 | | | V |
| VIL | SCL, SDA input low voltage | | | | 0.54 | V |
| T _{Active} | Time from power-on to ready to receive I ² C commands | | | 1.5 | | ms |

Note(s):

- Values are shown at the VDD pin and do not include current through the IR LED.
- This parameter indicates the supply current during periods of ALS integration. If Wait is enabled (WEN=1), the supply current is lower during the Wait period.
- Idle state occurs when PON=1 and all functions are not enabled.
- Sleep state occurs when PON = 0 and I²C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
- Digital pins: SDA, SCL, INT, are tolerant to a communication voltage up to 3.0V

Figure 7:
Electrical Characteristics of TMD3725

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|--|------------|------|-----|------|------|
| V _{DD} | Supply voltage | | 1.7 | 1.8 | 2.0 | V |
| V _{LEDA} | Supply voltage to LED anode ⁽¹⁾ | | 3.0 | 3.3 | 3.6 | V |
| | Voltage on pin with respect to ground; SDA, SCL, INT | | -0.3 | | 3.6V | |

Note(s):

- While the device is operational across the temperature range, performance will vary with temperature. Operational characteristics are at 25°C, unless otherwise noted.

Typical Operating Characteristics

Figure 8:
Optical Characteristics of TMD3725

| Parameter | Conditions | Clear Channel | | | Unit |
|--|--|---------------|------|------|---|
| | | Min | Typ | Max | |
| Re Irradiance responsivity Settings: AGAIN = 16x ATIME = 400ms | $\lambda_D = 465 \text{ nm LED}, 53.8 \mu\text{W}/\text{cm}^2$ | | 128 | | Count/ ($\mu\text{W}/\text{cm}^2$) |
| | $\lambda_D = 530 \text{ nm LED}, 43.9 \mu\text{W}/\text{cm}^2$ | | 161 | | |
| | $\lambda_D = 620 \text{ nm LED}, 37.5 \mu\text{W}/\text{cm}^2$ | | 191 | | |
| | Warm White LED, $45.6 \mu\text{W}/\text{cm}^2$ | | 161 | | |
| | Warm White LED, $45.6 \mu\text{W}/\text{cm}^2$ | 5950 | 7000 | 8050 | Counts |
| | $\lambda_D = 950 \text{ nm LED}, 21.1 \mu\text{W}/\text{cm}^2$ | | 1.5 | | Count/ ($\mu\text{W}/\text{cm}^2$) |

Figure 9:
ALS Optical Characteristics of TMD3725

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|------|-------|------|--------------|
| Integration time step size | | 2.68 | 2.78 | 2.90 | ms |
| Dark ADC count value | $E_e = 0 \mu\text{W}/\text{cm}^2$ AGAIN: 64x ATIME = 100ms (0xDC) | 0 | 1 | 3 | Counts |
| Gain scaling, relative to 1x gain setting | AGAIN = 4x | | 4 | | x |
| | AGAIN = 16x | | 16 | | |
| | AGAIN = 64x | | 64 | | |
| | AGAIN = 128x | | 128 | | |
| ADC noise | AGAIN = 16x | | 0.005 | | % full scale |

Figure 10:
Proximity Optical Characteristics of TMD3725

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|-----|-----|-----|--------|
| Part to part variation ⁽¹⁾ | Conditions: PGAIN = 2 (4x) PLDRIVE = 8 (54mA) PPULSE = 15 (16 pulses) PPULSE_LEN = 1 (8µs) d=23mm round target 30mm target distance | 75 | 100 | 125 | % |
| Response, absolute | Basic proximity measurement ⁽²⁾ Conditions: PGAIN = 2 (4x), PLDRIVE = 16 (102mA) PPULSE = 15 (16 pulses) PPULSE_LEN = 2 (16µs) Target material: 90% reflective surface of Kodak gray card Target Size: 100mm x 100mm Target Distance: 100mm | 128 | 160 | 192 | Counts |
| Response, no target after optical calibration | PGAIN = 2 (4x) ILED DRIVE = 16 (102mA) PPULSE = 16 (17 pulses) Pulse Length = 2 (16µs) | 0 | | 12 | |
| Noise/Signal ⁽³⁾ | PGAIN = 2 (4x) IRLED DRIVE = 8 (54mA) PPULSE = 15 (16 pulses) PPULSE_LEN = 1 (8µs) d=23mm round target 30mm target distance | | | 1 | % |

Note(s):

1. Production tested result is the average of 5 readings expressed relative to a calibrated response.
2. Representative result by characterization.
3. Production tested result is the average of 20 readings divided by the maximum proximity value 255.

Figure 11:
CRGB Optical Characteristics of TMD3725

| Parameter | Conditions | Red/Clear | | Green/Clear | | Blue/Clear | |
|---|------------------------------|-----------|--------------------|-------------------|-----|------------|--------------------|
| | | Min | Max | Min | Max | Min | Max |
| Color ADC count value ratio: color/clear | $\lambda_D = 465 \text{ nm}$ | 0% | 20% | 0% ⁽¹⁾ | 55% | 80% | 100% |
| | $\lambda_D = 525 \text{ nm}$ | 0% | 30% ⁽¹⁾ | 65% | 90% | 0% | 50% ⁽¹⁾ |
| | $\lambda_D = 615 \text{ nm}$ | 80% | 110% | 0% ⁽¹⁾ | 20% | 0% | 20% |
| | White LED, 2700K | 50% | 70% | 24% | 45% | 10% | 35% |

Note(s):

1. Not production tested.

Figure 12:
Spectral Responsivity of TMD3725

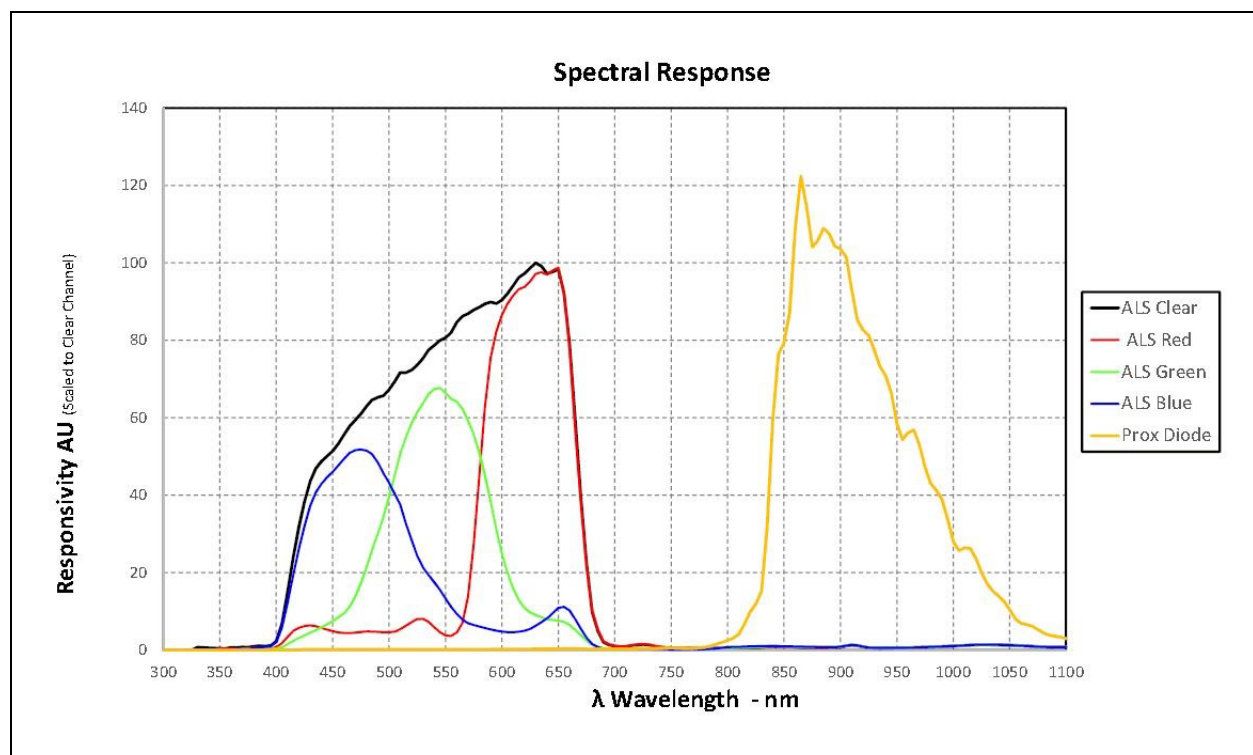


Figure 13:
Illuminance (Lux) vs Counts (Clear Channel) of TMD3725

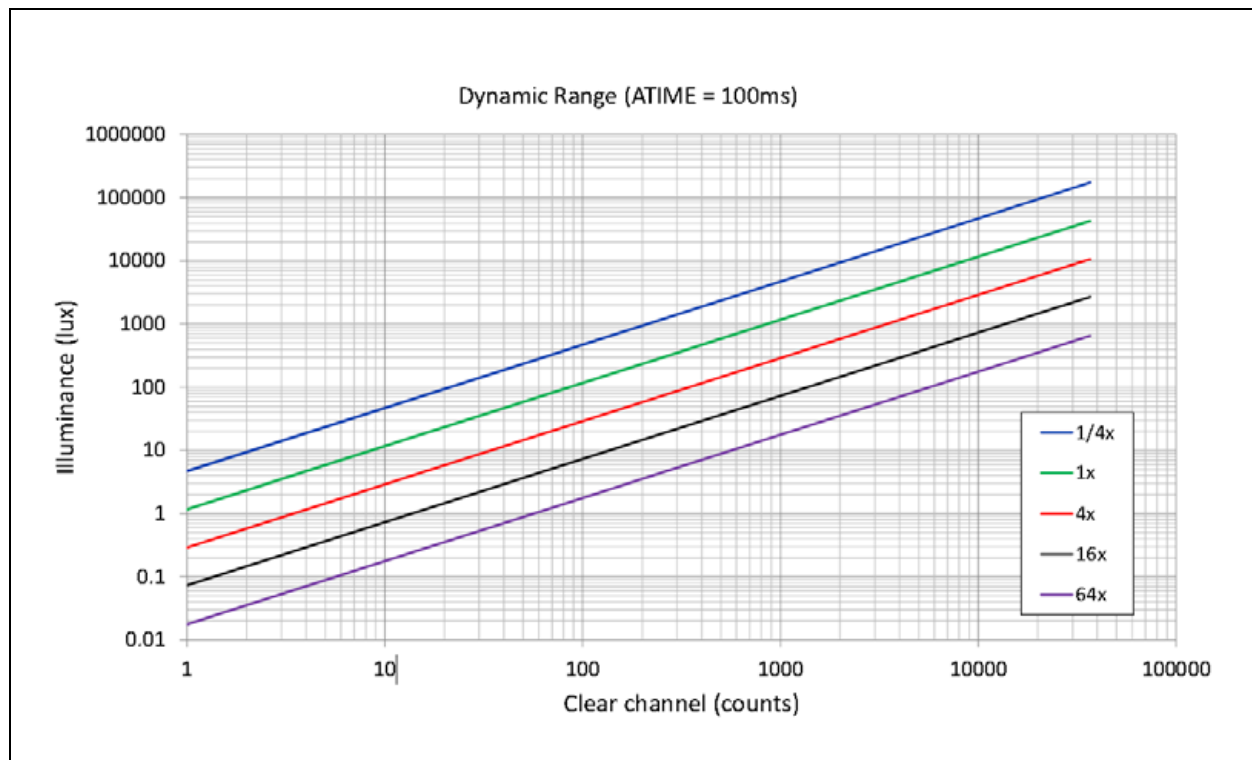


Figure 14:
Proximity Average Angular Response of TMD3725

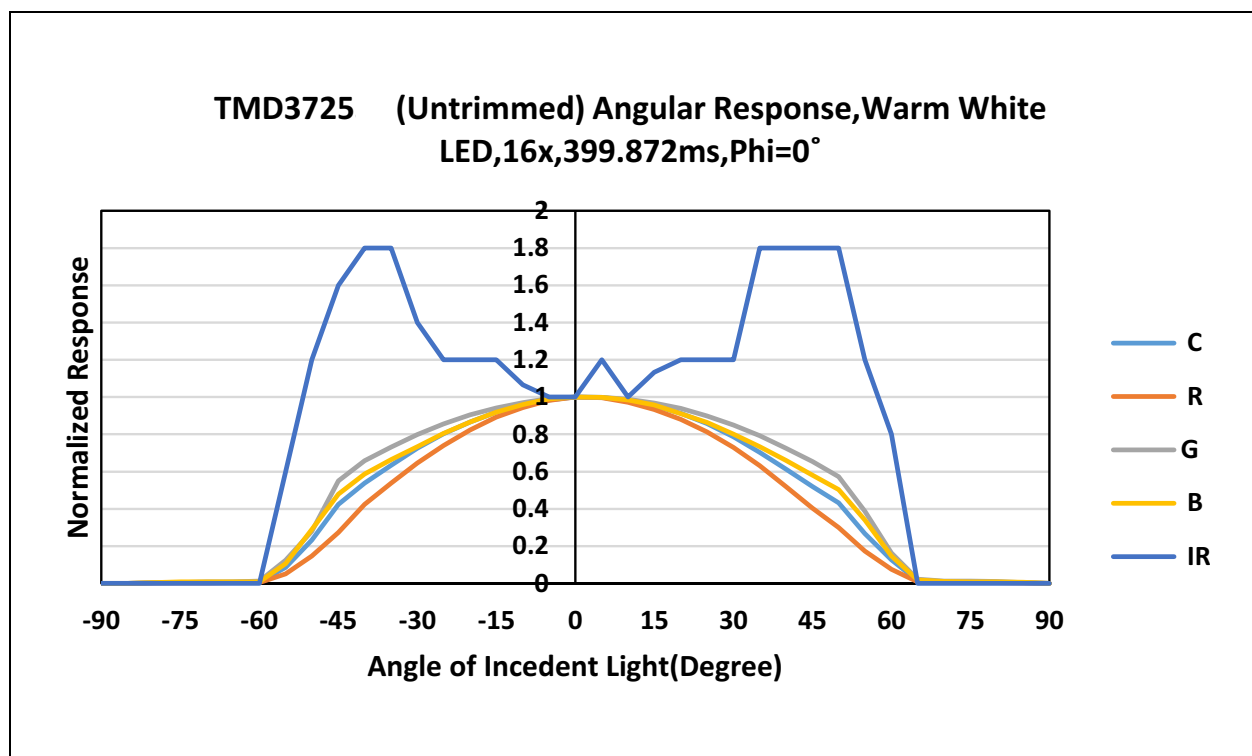
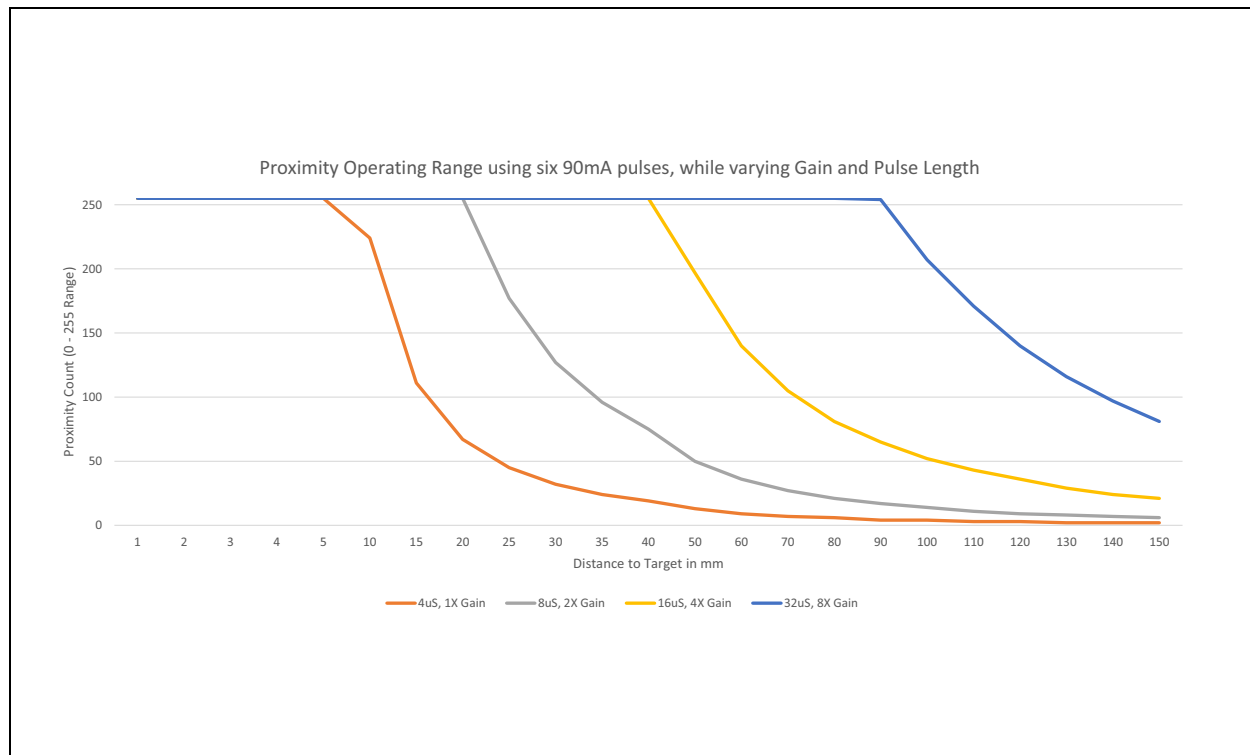


Figure 15:
Proximity Operation of TMD3725



Proximity Operation: By varying Gain, LED drive current, number of LED pulses and LED pulse duration the proximity detection range can be adjusted.

Detailed Description

Proximity

Proximity results are affected by three fundamental factors: the integrated IR LED emission, IR reception, and environmental factors, including target distance and surface reflectivity.

The IR reception signal path begins with IR detection from a photodiode and ends with the 8-bit proximity result in PDATA register. Signal from the photodiode is amplified, and offset adjusted to optimize performance. Offset correction or cross-talk compensation is accomplished by adjustment to the POFFSET register.

The analog circuitry of the device applies the offset value as a subtraction to the signal accumulation; therefore a positive offset value has the effect of decreasing the results.

Color and Ambient Light Sense

The color and ALS reception signal path begins as photodiodes receive filtered light and ends with 16-bit results. The IR photodiode primarily used for proximity sense, is multiplexed with the green channel's ADC to measure the IR content of ambient light. The color photodiodes are filtered with a UV and IR filters. The IR photodiode is filtered to receive only IR. Signal from the RGBC photodiodes simultaneously accumulate for a period of time set by the value in ATIME before the results are available. Measurement of IR must be done in a separate integration because it shares the ADC with the green photodiode. Gain is adjustable from 1x to 128 x to facilitate operation over a wide range of lighting conditions. Custom LUX equations are used to calculate the amount of ambient light, color temperature, as well as, determine the light type (e.g. LED, fluorescent, incandescent, etc.) using the ALS results.

I²C Characteristics

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and fast clock frequency modes with a chip address of 0x39. Read and Write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I²C bus is released).

During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address + 1.

I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESS_{WRITE}, REGISTER-ADDRESS, DATA BYTE(S), and STOP. Following each byte (9th clock pulse) the slave places an ACKNOWLEDGE/NOT-ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESS_{WRITE}, REGISTER-ADDRESS, START, CHIP-ADDRESS_{READ}, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9th clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

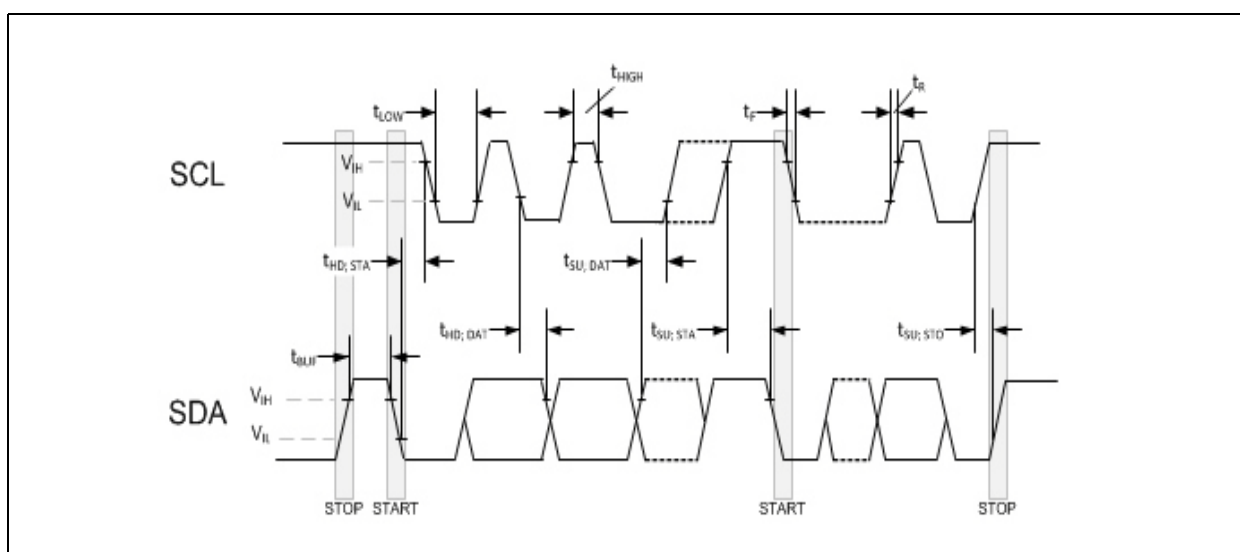
Alternately, if the previous I²C transaction was a Read, the internal register address buffer is still valid, allowing the transaction to proceed without “re”-specifying the register address. In this case the transaction consists of a START, CHIP-ADDRESS_{READ}, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9th clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at:

www.i2c-bus.org/references/

Timing Diagrams

Figure 16:
I²C Timing



Principles of Operation

System State Machine

An internal state machine provides system control of the ALS, proximity detection, and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a lowpower Sleep state. When a write on I²C bus to the Enable register (0x80) PON bit is set, the device transitions to the Idle state. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until a Proximity or ALS function is enabled. Once enabled, the device will execute the ALS, Proximity and Wait states in sequence as indicated in [Figure 17](#) and [Figure 18](#). Upon completion, the device will automatically begin a new ALS-Prox-Wait cycle as long as PON and either PEN or AEN remain enabled. If the Prox or ALS function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled, the device will transition to the Sleep state and remain in a low-power mode until an I²C command is received clearing the interrupts in the STATUS register. See Interrupts for additional information.

Figure 17:
Detailed State Diagram

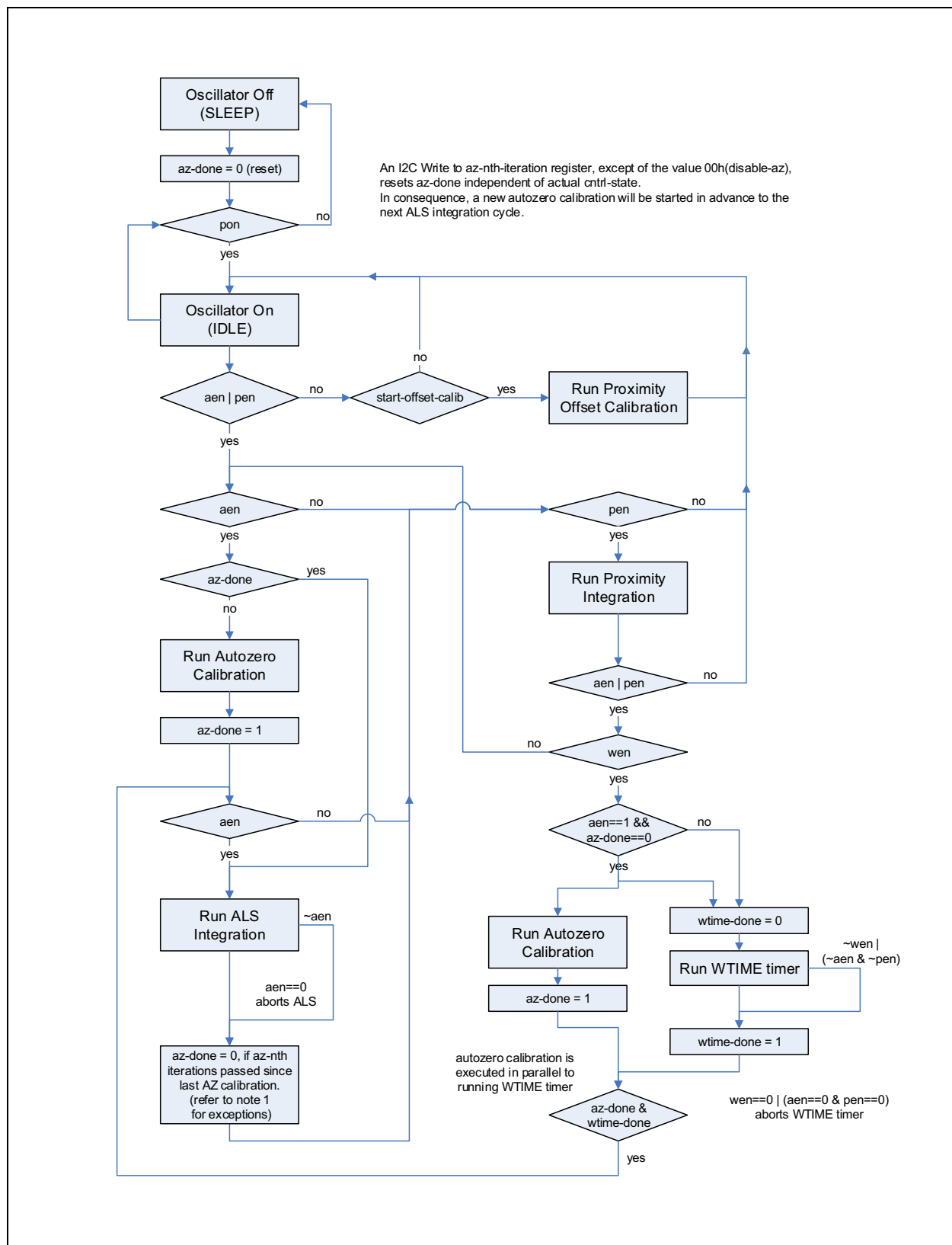
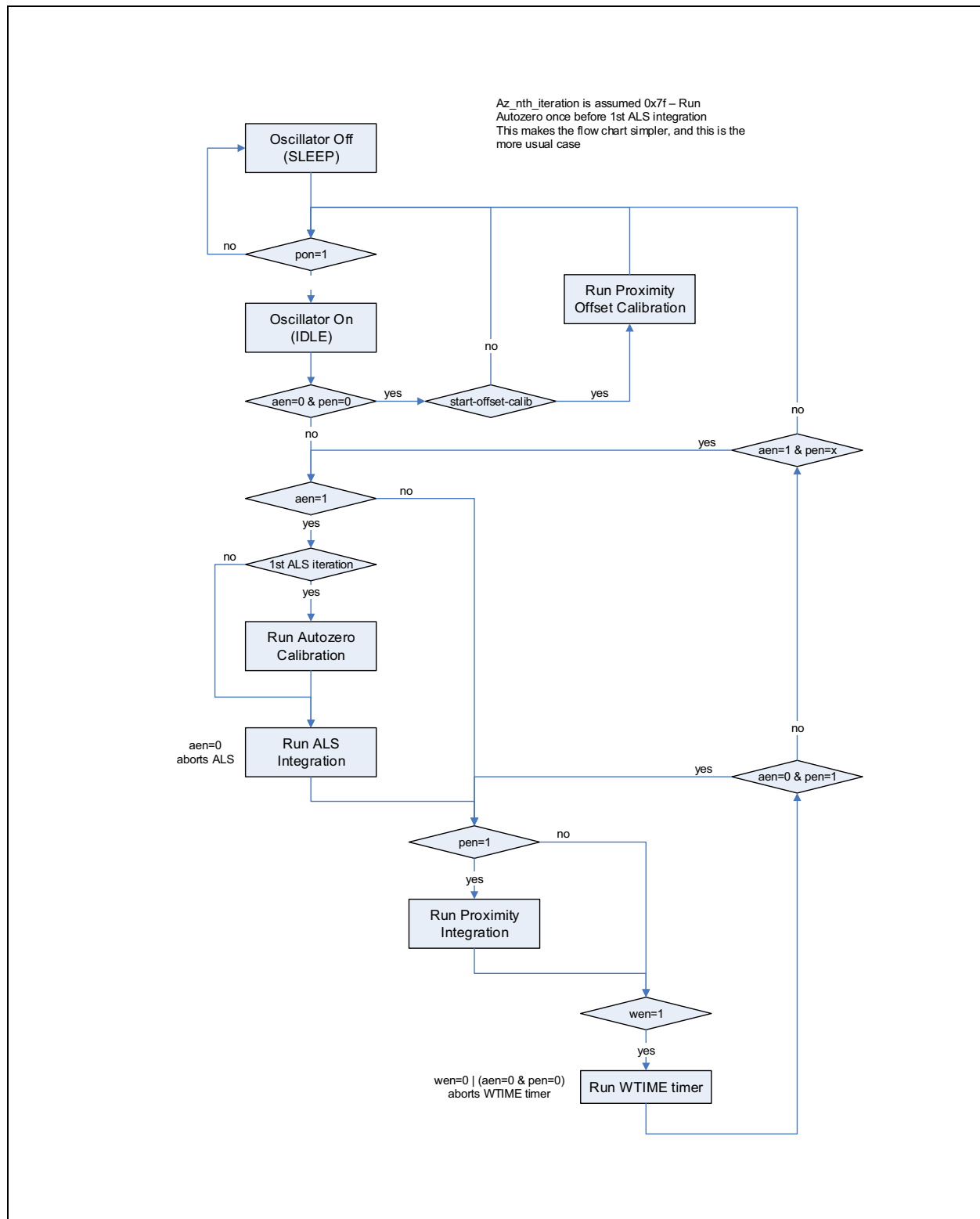


Figure 18:
Simplified State Diagram



Register Description

Register Overview

Figure 19:
Register Overview

| Addr | Name | <D7> | <D6> | <D5> | <D4> | <D3> | <D2> | <D1> | <D0> |
|------|-----------------------|------------|------|--------|---------|-------------|--------|-----------------|--------------|
| 0x80 | ENABLE | | | | | WEN | PEN | AEN | PON |
| 0x81 | ATIME | | | | | | | | |
| 0x82 | PTIME | | | | | | | | |
| 0x83 | WTIME | | | | | | | | |
| 0x84 | AILTL | | | | | | | | |
| 0x85 | AILTH | | | | | | | | |
| 0x86 | AIHTL | | | | | | | | |
| 0x87 | AIHTH | | | | | | | | |
| 0x88 | PILT | | | | | | | | |
| 0x8A | PIHT | | | | | | | | |
| 0x8C | PERS | PPERS | | | | APERS | | | |
| 0x8D | CFG0 | | | | | | WLONG | | |
| 0x8E | PCFG0 | PPULSE_LEN | | PPULSE | | | | | |
| 0x8F | PCFG1 | PGAIN | | | PLDRIVE | | | | |
| 0x90 | CFG1 | | | | | IR_TO_GREEN | | AGAIN | |
| 0x91 | REVID | | | | | | REV_ID | | |
| 0x92 | ID | ID | | | | | | | |
| 0x93 | STATUS | ASAT | PSAT | PINT | AIN | CINT | | PSAT_REFLECTIVE | PSAT_AMBIENT |
| 0x94 | CDATA1 | | | | | | | | |
| 0x95 | CDATAH | | | | | | | | |
| 0x96 | RDATA1 | | | | | | | | |
| 0x97 | RDATAH | | | | | | | | |
| 0x98 | GDATAL ⁽¹⁾ | | | | | | | | |
| 0x99 | GDATAH ⁽¹⁾ | | | | | | | | |

| Addr | Name | <D7> | <D6> | <D5> | <D4> | <D3> | <D2> | <D1> | <D0> |
|------|-----------|------------------------|-------|----------------------------|------|--------------------------------------|--------------|------|----------------------------|
| 0x9A | BDATAI | | | | | | | | |
| 0x9B | BDATAH | | | | | | | | |
| 0x9C | PDATA | | | | | | | | |
| 0x9F | CFG2 | | | | | | AGAINL | | |
| 0xAB | CFG3 | INT_ READ_ CLEAR | | | SAI | | | | |
| 0xC0 | POFFSETL | | | | | | | | |
| 0xC1 | POFFSETH | | | | | | | | POFFSET_ SIGN |
| 0xD7 | CALIB | | | ELECTRICAL_ CALIBRATION | | | | | START_ OFFSET_ CALIB |
| 0xD9 | CALIBCFG | BINSRCH_TARGET | | | | DCAVG_ AUTO_ OFFSET_ ADJUST | PRX_DATA_AVG | | |
| 0xDC | CALIBSTAT | | | | | | | | CALIB_ FINISHED |
| 0xDD | INTENAB | ASIEN | PSIEN | PIEN | AIEN | CIEN | | | |

Note(s):

- Address 0x98 and 0x99 contain the results for both Green and IR photodiodes as controlled by the Green/IR MUX.

Detailed Register Description

Enable Register (Address 0x80)

Figure 20:
Enable Register

| Addr: 0x80 | | Enable | | |
|------------|----------|---------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:4 | RESERVED | 0 | RW | Reserved. |
| 3 | WEN | 0 | RW | This bit activates the wait feature. Active high. |
| 2 | PEN | 0 | RW | This bit activates the proximity detection. Active high. |
| 1 | AEN | 0 | RW | This bit activates the ALS function. Active high. *Set AEN=1 and PON=1 in the same command to ensure auto-zero function is run prior to the first measurement. |
| 0 | PON | 0 | RW | This field activates the internal oscillator and ADC channels. Active high. |

Before activating AEN or PEN, preset each applicable operating mode registers and bits.

ATIME Register (Address 0x81)

Figure 21:
ATIME Register

| Addr: 0x81 | | ATIME | | | | | |
|------------|----------|---------|--------|--|--------------------|------------------|-------------------|
| Bit | Bit Name | Default | Access | Bit Description | | | |
| 7:0 | ATIME | 0x00 | RW | ALS/Color value that specifies the integration time in 2.81ms intervals. 0x00 indicates 2.8ms. The maximum ALS value depends on the integration time. For every 2.81ms, the maximum value increases by 1024. This means that to be able to reach ALS full scale, the integration time has to be at least 64*2.8ms. | | | |
| | | | | Value | Integration Cycles | Integration Time | Maximum ALS Value |
| | | | | 0x00 | 1 | 2.8ms | 1023 |
| | | | | 0x01 | 2 | 5.6ms | 2047 |
| | | | | ... | ... | ... | ... |
| | | | | 0x3F | 64 | 180ms | 65535 |
| | | | | ... | ... | ... | ... |
| | | | | 0xFF | 256 | 719ms | 65535 |

The ATIME register controls the integration time of the ALS ADCs. The timer is implemented with a down counter with 0x00 as the terminal count. The timer is clocked at a 2.8ms nominal rate. Loading 0x00 will generate a 2.8ms integration time, loading 0x01 will generate a 5.6ms integration time, and so forth. The RC oscillator runs at 8MHz nominal rate. This gets divided by 11 to generate the integration clock of 727kHz. One count in ATIME (nominal 2.8ms) are 2.81ms. This is 2048 integration clock cycles: $125\text{ns} \times 11 \times 8 \times 256 = 2.81\text{ms}$.

PTIME Register (Address 0x82)

Figure 22:
PTIME Register

| Addr: 0x82 | | PRATE | | | |
|------------|----------|---------|--------|--|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:0 | PTIME | 0x1F | RW | This register defines the duration of 1 Prox Sample, which is $(PTIME + 1) \times 88\mu\text{s}$. | |

WTIME Register (Address 0x83)**Figure 23:**
WTIME Register

| Addr: 0x83 | | WTIME | | | | |
|------------|----------|---------|--------|---|------------|----------------|
| Bit | Bit Name | Default | Access | Bit Description | | |
| 7:0 | WTIME | 0x00 | RW | Value that specifies the wait time between ALS cycles in 2.81ms increments. | | |
| | | | | Value | Increments | Wait Time |
| | | | | 0x00 | 1 | 2.8ms (33.8ms) |
| | | | | 0x01 | 2 | 5.6ms (67.6ms) |
| | | | | ... | ... | ... |
| | | | | 0x3F | 64 | 180ms (2.16s) |
| | | | | ... | ... | ... |
| | | | | 0xFF | 256 | 719ms (8.65s) |

The wait timer is implemented using a down counter.
 Wait time = (value + 1) x 2.8ms. If WLONG is enabled then
 Wait time = (value + 1) x 2.8ms x 12.

AILTL Register (Address 0x84)**Figure 24:**
AILTL Register

| Addr: 0x84 | | AILTL | | |
|------------|----------|---------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | AILTL | 0x00 | RW | This register sets the low byte of the LOW ALS threshold. |

The Clear (C) channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.

AILTH Register (Address 0x85)

Figure 25:
AILTH Register

| Addr: 0x85 | | AILTH | | |
|------------|----------|---------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | AILTH | 0x00 | RW | This register sets the high byte of the LOW ALS threshold. |

The Clear (C) channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.

The contents of the AILTH and AILTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is below the AILTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.

When setting the 16-bit ALS threshold AILTL must be written first, immediately followed by AILTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

AIHTL Register (Address 0x86)

Figure 26:
AIHTL Register

| Addr: 0x86 | | AIHTL | | |
|------------|----------|---------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | AIHTL | 0x00 | RW | This register sets the low byte of the HIGH ALS threshold. |

The Clear (C) channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.

The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert. When setting the 16-bit ALS threshold AIHTL must be written first, immediately followed by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

AIHTH Register (Address 0x87)**Figure 27:**
AIHTH Register

| Addr: 0x87 | | AIHTH | | |
|------------|----------|---------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | AIHTH | 0x00 | RW | This register sets the high byte of the HIGH ALS threshold. |

The Clear (C) channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.

The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.

When setting the 16-bit ALS threshold AIHTL must be written first, immediately follow by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

PILT Register (Address 0x88)**Figure 28:**
PILT Register

| Addr: 0x88 | | PILT | | |
|------------|----------|---------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | PILT | 0x00 | RW | This register sets the Proximity ADC channel low threshold. |

The proximity channel is compared against low-going 8-bit threshold value set by PILT.

If the value generated by the proximity channel is below the PILT threshold and the PPERS value is reached, the PINT bit is asserted. If PIEN is set, then the INT pin will also assert.

PIHT Register (Address 0x8A)

Figure 29:
PIHT Register

| Addr: 0x8A | | PIHT | | |
|------------|----------|---------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | PIHT | 0x00 | RW | This register sets the proximity ADC channel high threshold. |

The proximity channel is compared against high-going 8-bit threshold value set by PIHT.
If the value generated by the proximity channel is above the PIHT threshold and the PPERS value is reached, the PINT bit is asserted. If PIEN is set, then the INT pin will also assert.

PERS Register (Address 0x8C)

Figure 30:
PERS Register

| Addr: 0x8C | | PERS | | | |
|------------|----------|---------|--------|--|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:4 | PPERS | 0 | RW | This register sets the proximity persistence filter. | |
| | | | | Value | Interrupt |
| | | | | 0 | Every proximity cycle |
| | | | | 1 | Any value outside PILT/PIHT thresholds |
| | | | | 2 | 2 consecutive proximity values out of range |
| | | | | 3 | 3 consecutive proximity values out of range |
| | | | | ... | |
| | | | | 15 | 15 consecutive proximity values out of range |

| Addr: 0x8C | | PERS | | | |
|------------|----------|---------|--------|--|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 3:0 | APERS | 0 | RW | This register sets the ALS persistence filter. | |
| | | | | 0 | Every ALS cycle |
| | | | | 1 | Any value outside ALS thresholds |
| | | | | 2 | 2 consecutive ALS values out of range |
| | | | | 3 | 3 consecutive ALS values out of range |
| | | | | 4 | 5 consecutive ALS values out of range |
| | | | | 5 | 10 consecutive ALS values out of range |
| | | | | 6 | 15 consecutive ALS values out of range |
| | | | | 7 | 20 consecutive ALS values out of range |
| | | | | ... | ... |
| | | | | 13 | 50 consecutive ALS values out of range |
| | | | | 14 | 55 consecutive ALS values out of range |
| | | | | 15 | 60 consecutive ALS values out of range |

The frequency of consecutive proximity channel results outside of threshold limits are counted; this count value is compared against the PPEARS value. If the counter is equal to the PPEARS value an interrupt is asserted. Any time a proximity channel result is inside the threshold values the counter is cleared. The frequency of consecutive clear channel results outside of threshold limits are counted; this count value is compared against the APEARS value. If the counter is equal to the APERS setting an interrupt is asserted. Any time a clear channel result is inside the threshold values the counter is cleared.

CFG0 Register (Address 0x8D)

Figure 31:
CFG0 Register

| Addr: 0x8D | | CFG0 | | |
|------------|----------|---------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:3 | Reserved | 10000 | RW | This field must be set to the default value. |
| 2 | WLONG | 0 | RW | When Wait Long is asserted the wait period as set by WTIME is increased by a factor of 12. |
| 1:0 | Reserved | 0 | RW | This field must be set to the default value. |

The wait timer is implemented using a down counter.
Wait time = (value +1) x 2.8ms. If WLONG is enabled then
Wait time = (value +1) x 2.8ms x 12.

PCFG0 Register (Address 0x8E)**Figure 32:**
PCFG0 Register

| Addr: 0x8E | | PCFG0 | | | |
|------------|------------|---------|--------|---|--------------------------|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:6 | PPULSE_LEN | 01 | RW | Proximity pulse length | |
| | | | | Value | Pulse Length |
| | | | | 0 | 4μs |
| | | | | 1 | 8μs |
| | | | | 2 | 16μs |
| | | | | 3 | 32μs |
| 5:0 | PPULSE | 001111 | RW | Maximum number of pulses in a single proximity cycle. | |
| | | | | Value | Maximum Number of Pulses |
| | | | | 0 | 1 |
| | | | | 1 | 2 |
| | | | | 2 | 3 |
| | | | | ... | ... |
| | | | | 63 | 64 |

The PPULSE_LEN field sets the width of all IR LED pulses within the proximity cycle. Longer pulses result in increased proximity range and typically result in less electrical noise generated in the analog front end. However, a setting of 8μs is recommended because less cumulative noise is generated during a proximity cycle.

The PPULSE field sets the maximum number of IR LED pulses that may occur in a proximity cycle. The proximity engine will automatically continue to add IR LED pulses, up to the value set in PPULSE or if a near-saturation condition occurs.

The dynamic range of the sensor is automatically adjusted to detect distant targets as well as prevent saturation from close targets.

This operation also reduces power consumption because proximity integration period is automatically shortened when a target is either too close or far from the sensor.

PCFG1 Register (Address 0x8F)

Figure 33:
PCFG1 Register

| Addr: 0x8F | | PCFG1 | | | |
|------------|----------|---------|--------|--|-------------|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:6 | PGAIN | 10 | RW | This field sets the gain of the proximity IR sensor. | |
| | | | | Value | Gain |
| | | | | 0 | 1x |
| | | | | 1 | 2x |
| | | | | 2 | 4x |
| | | | | 3 | 8x |
| 5 | Reserved | 0 | RW | Reserved | |
| 4:0 | PLDRIVE | 0 | RW | This field sets the drive strength of the IR LED current. Values are approximate; actual current through LED is factory trimmed to normalize IR intensity. | |
| | | | | Value | LED Current |
| | | | | 0 | 6mA |
| | | | | 1 | 12mA |
| | | | | i _{LED} = 6(PLDRIVE +1) mA | |
| | | | | 30 | 186mA |
| | | | | 31 | 192mA |

CFG1 Register (Address 0x90)**Figure 34:**
CFG1 Register

| Addr: 0x90 | | CFG1 | | | |
|------------|-------------|---------|--------|--|-------------|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:4 | Reserved | 0000 | RW | Reserved | |
| 3 | IR_TO_GREEN | 0 | RW | If set high, the IR (Proximity) photodiode is switched into the Green channel's data converter. GDATAL/H register will report IR content. Green photodiode is not connected. | |
| 2 | Reserved | 0 | RW | Reserved | |
| 1:0 | AGAIN | 00 | RW | This field sets the gain of the ALS/Color sensor. | |
| | | | | Value | LED Current |
| | | | | 0 | 1x |
| | | | | 1 | 4x |
| | | | | 2 | 16x |
| | | | | 3 | 64x |

REVID Register (Address 0x91)**Figure 35:**
REVID Register

| Addr: 0x91 | | REVID | | |
|------------|----------|---------|--------|------------------------|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:3 | Reserved | 00000 | RO | Reserved |
| 2:0 | REV_ID | Rev | RO | Device revision number |

ID Register (Address 0x92)

Figure 36:
ID Register

| Addr: 0x92 | | ID | | |
|------------|----------|---------|--------|-----------------------------|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:2 | ID | 111001 | RO | Device type identification. |
| 1:0 | Reserved | 01 | RO | Reserved |

Status Register (Address 0x93)

Figure 37:
Status Register

| Addr: 0x93 | | Status Register | | |
|------------|-----------------|-----------------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7 | ASAT | 0 | R, SC | The Analog Saturation flag signals that the ALS/Color results may be unreliable due to saturation of the AFE. |
| 6 | PSAT | 0 | R, SC | The Proximity Saturation flag indicates that an ambient- or reflective-saturation event occurred during a previous proximity cycle. |
| 5 | PINT | 0 | R, SC | The Proximity Interrupt flag indicates that proximity results have exceeded thresholds and persistence settings. |
| 4 | AINT | 0 | R, SC | The ALS Interrupt flag indicates that ALS/Color results (clear channel) have exceeded thresholds and persistence settings. |
| 3 | CINT | 0 | R, SC | The Calibration Interrupt flag indicates that calibration has completed. |
| 2 | Reserved | 0 | R, SC | Reserved |
| 1 | PSAT_REFLECTIVE | 0 | R, SC | The Reflective Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR LED active portion of proximity integration. |
| 0 | PSAT_AMBIENT | 0 | R, SC | The Ambient Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR LED inactive portion of proximity integration. |

All flags in this register can be cleared by setting the bit high. Alternatively, if the CFG3.int_read_clear bit is set, then simply reading this register automatically clears all eight flags.

CDATAL Register (Address 0x94)**Figure 38:**
CDATAL Register

| Addr: 0x94 | | CDATAL | | |
|------------|----------|---------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | CDATAL | 0x00 | RO | This register contains the low byte of the 16-bit clear channel data. |

CDATAH Register (Address 0x95)**Figure 39:**
CDATAH Register

| Addr: 0x95 | | CDATAH | | |
|------------|----------|---------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | CDATAH | 0x00 | RO | This register contains the high byte of the 16-bit clear channel data. |

RDATAL Register (Address 0x96)**Figure 40:**
RDATAL Register

| Addr: 0x96 | | RDATAL | | |
|------------|----------|---------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | RDATAL | 0x00 | RO | This register contains the low byte of the 16-bit red channel data. |

RDATAH Register (Address 0x97)**Figure 41:**
RDATAH Register

| Addr: 0x97 | | RDATAH | | |
|------------|----------|---------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | RDATAH | 0x00 | RO | This register contains the high byte of the 16-bit red channel data. |

GDATAL Register (Address 0x98)

Figure 42:
GDATAL Register

| Addr: 0x98 | | GDATAL | | |
|------------|----------|---------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | GDATAL | 0x00 | RO | This register contains the low byte of the 16-bit green channel data. |

GDATAL Register: This register also contains the IR result as set by the Green/IR MUX.

GDATAH Register (Address 0x99)

Figure 43:
GDATAH Register

| Addr: 0x99 | | GDATAH | | |
|------------|----------|---------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | GDATAH | 0x00 | RO | This register contains the high byte of the 16-bit green channel data. |

GDATAH Register: This register also contains the IR result as set by the Green/IR MUX.

BDATAH Register (Address 0x9A)

Figure 44:
BDATAL Register

| Addr: 0x9A | | BDATAL | | |
|------------|----------|---------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | BDATAL | 0x00 | RO | This register contains the low byte of the 16-bit blue channel data. |

BDATAH Register (Address 0x9B)

Figure 45:
BDATAH Register

| Addr: 0x9B | | BDATAH | | |
|------------|----------|---------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | BDATAH | 0x00 | RO | This register contains the high byte of the 16-bit blue channel data. |

PDATA Register (Address 0x9C)**Figure 46:**
PDATA Register

| Addr: 0x9C | | PDATA | | |
|------------|----------|---------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | PDATA | 0x00 | RO | This register contains the 8-bit proximity channel data. |

CFG2 Register (Address 0x9F)**Figure 47:**
CFG2 Register

| Addr: 0x9F | | CFG2 | | |
|------------|----------|---------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:3 | Reserved | 0 | RW | Reserved |
| 2 | AGAINL | 1 | RW | This bit adjusts the overall ALS gain factor. Reset to 0 causes the overall gain to be divided by 2. ALS gain will be unaffected when set to 1. |
| 1:0 | Reserved | 0 | RW | Reserved |

The ALS gain can be adjusted using by setting the two AGAIN bits as well as the AGAINL bit which yields an overall range from $\frac{1}{2}$ x to 64x.

Figure 48:
AGAIN Range

| AGAIN[1] | AGAIN[0] | AGAINL | Overall ALS Gain |
|----------|----------|--------|------------------|
| 0 | 0 | 0 | $\frac{1}{2}$ |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 8 |
| 1 | 0 | 1 | 16 |
| 1 | 1 | 0 | 32 |
| 1 | 1 | 1 | 64 |

CFG3 Register (Address 0xAB)

Figure 49:
CFG3 Register

| Addr: 0xAB | | CFG3 | | | |
|------------|----------------|---------|--------|--|------------|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7 | INT_READ_CLEAR | 0 | RW | If the Interrupt-Clear-by-Read bit is set, then all flag bits in the STATUS register will be reset whenever the STATUS register is read over I ² C. | |
| 6:5 | Reserved | 0 | RW | Reserved | |
| 4 | SAI | 0 | RW | The Sleep After Interrupt bit is used to place the device into a low power mode upon an interrupt pin assertion. | |
| | | | | PON | SAI |
| | | | | 0 | X |
| | | | | 1 | 0 |
| | | | | 1 | 1 |
| 3:0 | Reserved | 0xC | RW | 1 | 0 |
| | | | | 1 | 1 |

The SAI bit sets the device operational mode following the completion of an ALS or proximity cycle. If AINT and AIEN are both set or if PINT and PIEN are both set, causing an interrupt on the INT pin, and the SAI bit is set, then the oscillator will deactivate. The Device will appear as if PON = 0, however, PON will read as 1. The device can only be reactivated (oscillator enabled) by clearing the interrupts in the STATUS register.

POFFSETL Register (Address 0xC0)**Figure 50:**
POFFSETL Register

| Addr: 0xC0 | | POFFSETL | | |
|------------|----------|----------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | POFFSETL | 0x00 | RW | This register contains the magnitude portion of proximity offset adjust value. |

Typically, optical and/or electrical crosstalk negatively influence proximity operation and results. The POFFSETL/POFFSETH registers provide a mechanism to remove system crosstalk from the proximity data. POFFSETL and POFFSETH contains the magnitude and sign of a value which adjusts PDATA is generated in the AFE. An offset value in the range of ± 127 is possible.

POFFSETH Register (Address 0xC1)**Figure 51:**
POFFSETH Register

| Addr: 0xC1 | | POFFSETH | | |
|------------|--------------|----------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:1 | Reserved | 0 | RW | Reserved |
| 0 | POFFSET_SIGN | 0 | RW | This register contains the sign portion of proximity offset adjust value. |

Typically, optical and/or electrical crosstalk negatively influence proximity operation and results. The POFFSETL/POFFSETH registers provide a mechanism to remove system crosstalk from the proximity data. POFFSETL and POFFSETH contains the magnitude and sign of a value which adjusts PDATA is generated in the AFE. An offset value in the range of ± 127 is possible.

CALIB Register (Address 0xD7)

Figure 52:
CALIB Register

| Addr: 0xD7 | | CALIB | | |
|------------|------------------------|---------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:6 | Reserved | 0 | RO | Reserved |
| 5 | ELECTRICAL_CALIBRATION | 0 | RW | Selects proximity calibration type. 1=Electrical offset only. 0= Calibration compensates for electrical and optical crosstalk. |
| 4:1 | Reserved | 0 | RW | Reserved |
| 0 | START_OFFSET_CALIB | 0 | RW | Set to 1 to start a calibration sequence. |

Proximity response in systems with electrical and optical crosstalk may be improved by using the calibration feature. Optical crosstalk is caused when the photodiode receives a small portion of the LED IR which was unintentionally reflected by a surface other than the target. Electrical offset is caused by electrical disturbance in the sensor AFE, and also influences the proximity result. The calibration routine adjusts the value in registers C0 and C1 until the proximity result is as close to BINSRCH_TARGET as possible without becoming zero.

Optical and electrical calibration function identically, except that during an electrical calibration the proximity photodiode is disconnected from the AFE.

Upon power-up, the device always automatically performs an electrical calibration. However, an electrical calibration can be initiated anytime by setting the ELECTRICAL_CALIBRATION and START_OFFSET_CALB bits.

To perform an optical (and electrical) calibration do not set the ELECTRICAL_CALIBRATION bit when setting the START_OFFSET_CALIB. The CINT flag will assert after calibration has finished.

Upon completion proximity offset registers are automatically loaded with calibration result.

CALIBCFG Register (Address 0xD9)**Figure 53:**
CALIBCFG Register

| Addr: 0xD9 | | CALIBCFG | | | |
|------------|-----------------|----------|--------|--|--------------|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:5 | BINSRCH_TARGET | 010 | RW | Proximity Result Target | |
| | | | | Value | PDATA Target |
| | | | | 0 | 0 |
| | | | | 1 | 1 |
| | | | | 2 | 3 |
| | | | | 3 | 7 |
| | | | | 4 | 15 |
| | | | | 5 | 31 |
| | | | | 6 | 63 |
| | | | | 7 | 127 |
| 4 | Reserved | 0 | RW | Reserved | |
| 3 | AUTO_OFFSET_ADJ | 0 | RW | The Proximity Auto Offset Adjust bit causes the value in POFFSETL register to decrement when PDATA equals zero at the completion of the proximity cycle. | |
| 2:0 | PROX_AVG | 0 | RW | The Proximity Averaging field defines the number of ADC samples collected and averaged during a cycle which become the proximity result. | |
| | | | | Value | Sample Size |
| | | | | 0 | Disable |
| | | | | 1 | 2 |
| | | | | 2 | 4 |
| | | | | 3 | 8 |
| | | | | 4 | 16 |
| | | | | 5 | 32 |
| | | | | 6 | 64 |
| | | | | 7 | 128 |

The binary search target field is used by the calibration feature to set the baseline value for PDATA when no target is present. For example, calibration of a device in open air, with no target,

and BINSEARCH_TARGET setting of 4 causes the PDATA value will be approximately 15 counts. This feature is useful because it forces PDATA result to always be above zero.

The PROX_AVG field sets the number of ADC samples that are averaged to calculate the PDATA result.

CALIBSTAT Register (Address 0xDC)

Figure 54:
CALIBSTAT Register

| Addr: 0xDC | | CALIBSTAT | | |
|------------|----------------|-----------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:1 | Reserved | 0 | RW | Reserved |
| 0 | CALIB_FINISHED | 0 | RW | This flag indicates that calibration has finished. It can only be cleared by setting this bit high. |

INTENAB Register (Address 0xDD)

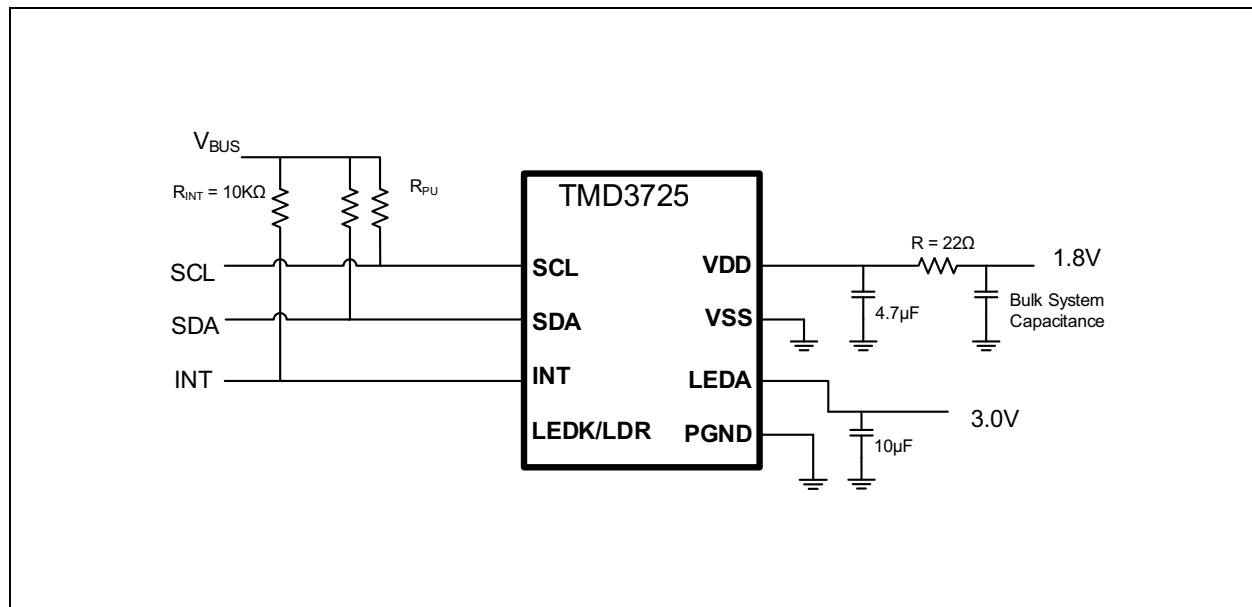
Figure 55:
INTENAB Register

| Addr: 0xDD | | INTENAB | | |
|------------|----------|---------|--------|---------------------------------------|
| Bit | Bit Name | Default | Access | Bit Description |
| 7 | ASIEN | 0 | RW | ALS Saturation Interrupt Enable |
| 6 | PSIEN | 0 | RW | Proximity Saturation Interrupt Enable |
| | PIEN | 0 | RW | Proximity Interrupt Enable |
| 4 | AIEN | 0 | RW | ALS/Color Interrupt Enable |
| 3 | CIEN | 0 | RW | Calibration Interrupt Enable |
| 2:0 | Reserved | 0 | RW | Reserved |

Application Information

Schematic

Figure 56:
Typical Applications Circuit



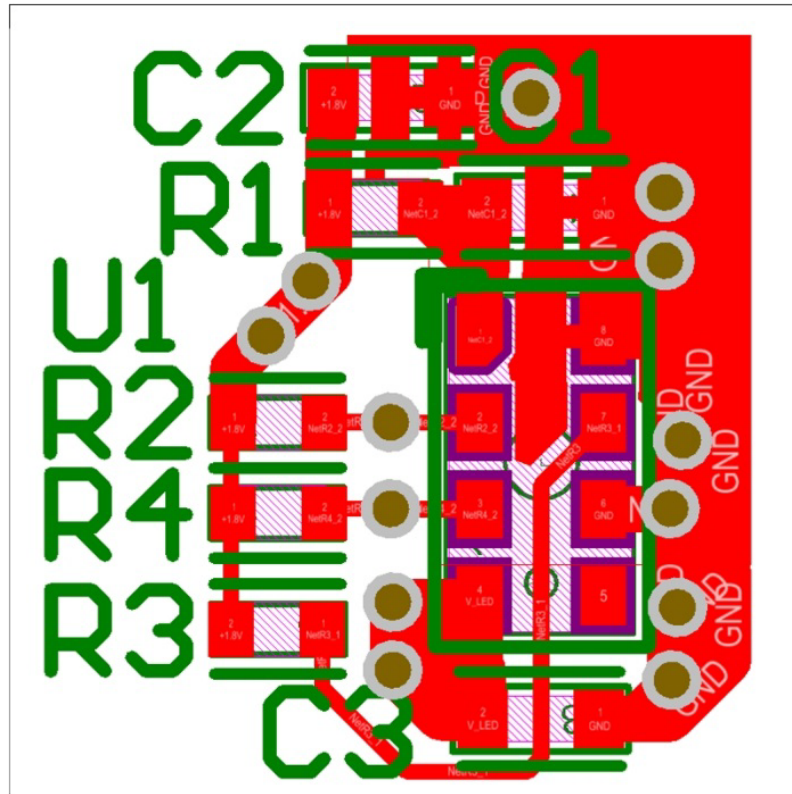
Typical Applications Circuit: It is important to place the 4.7μF (VDD) and 10μF (LEDA) capacitors at the package pins.

Note(s):

1. Place the 4.7μF and 10μF LEDA capacitors within 5mm of the module.
2. The value of the I²C pull up resistors R_{PU} should be based on the 1.8V bus voltage, system bus speed and trace capacitance.
3. The bulk capacitor can affect the stability of a regulated supply output and should be chosen with the regulator characteristics in mind.
4. VSS and PGND should be connected to the same solid ground plane as close to the device as possible.

PCB Layout

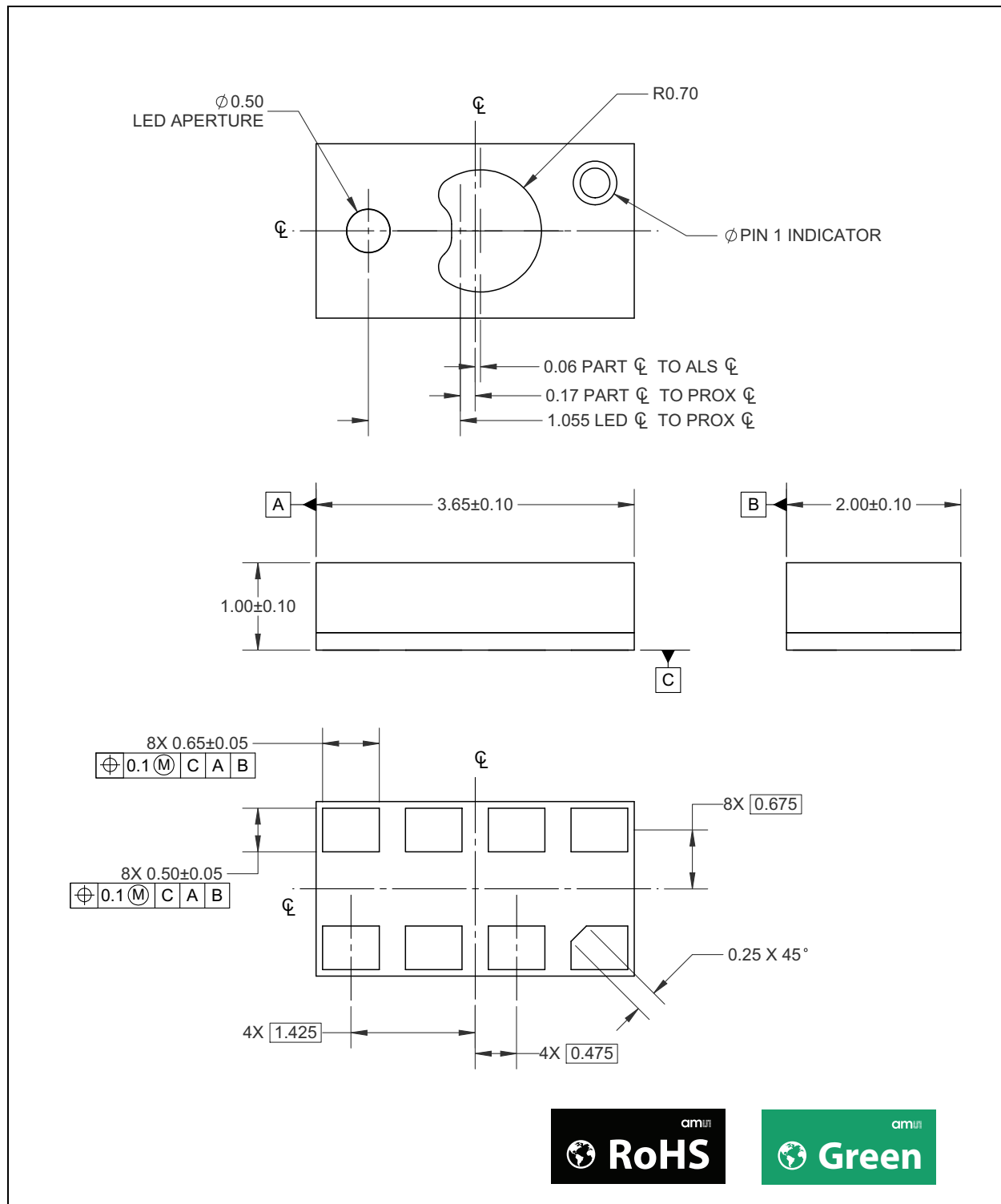
Figure 57:
PCB Layout



The dominant factor governing device performance is the component placement, not necessarily component value. The placement of the decoupling capacitor, C1, is the most critical. Place the component on the same side of PCB as device as shown in the figure above. Make connection as close as possible to minimize series inductance and resistance. This is critical.

Package Drawings & Markings

Figure 58:
Package Drawings

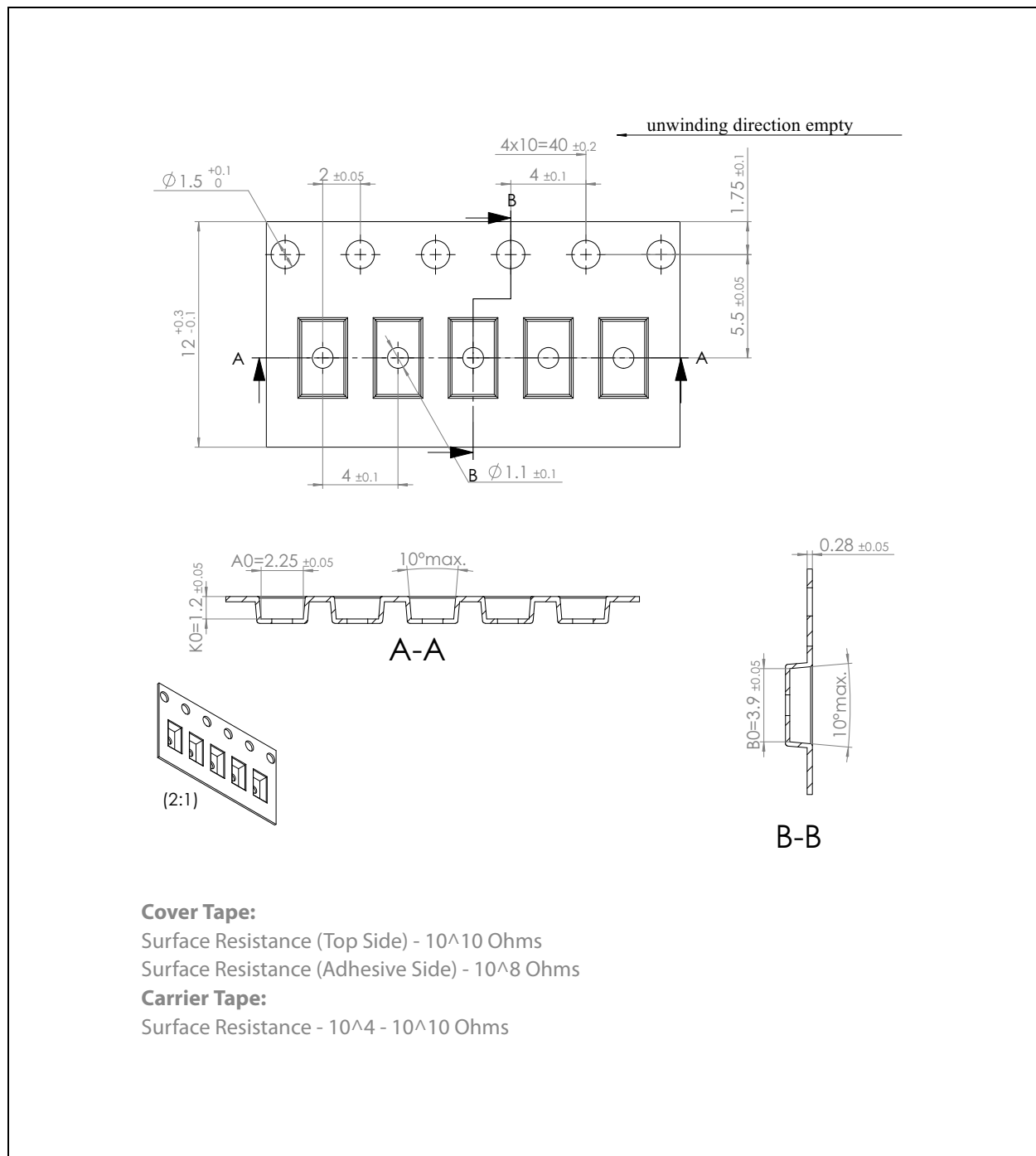


Note(s):

1. All linear dimensions are in millimeters.
2. Contact finish is Au.
3. This package contains no lead (Pb).
4. This drawing is subject to change without notice.

Tape & Reel Information

Figure 60:
Tape and Reel Information



Note(s):

1. All linear dimensions are in millimeters.
2. For missing tolerances and dimensions, refer to EIA-481.

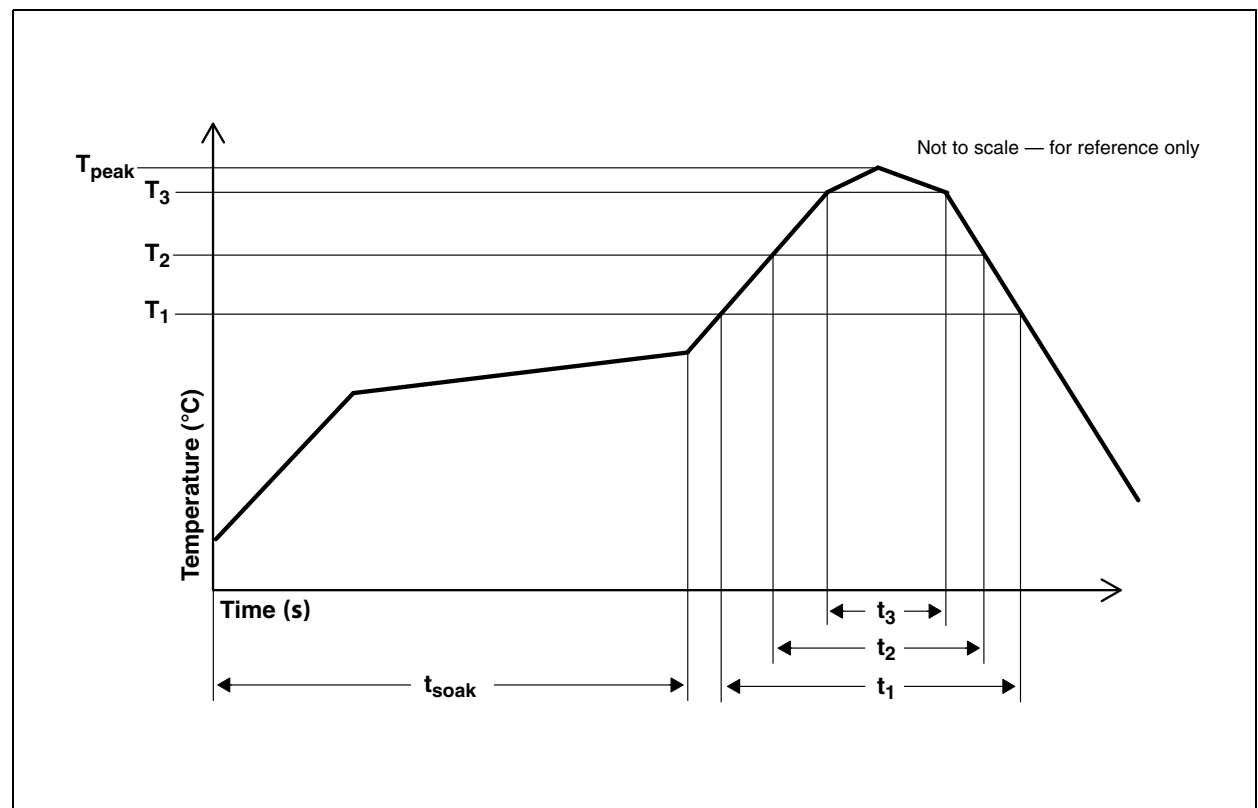
Soldering & Storage Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 61:
Solder Reflow Profile

| Parameter | Reference | Device |
|--|------------|----------------|
| Average temperature gradient in preheating | | 2.5°C/s |
| Soak time | t_{SOAK} | 2 to 3 minutes |
| Time above 217°C (T_1) | t_1 | Max 60s |
| Time above 230°C (T_2) | t_2 | Max 50s |
| Time above $T_{peak} - 10^\circ\text{C}$ (T_3) | t_3 | Max 10s |
| Peak temperature in reflow | T_{peak} | 260°C |
| Temperature gradient in cooling | | Max - 5°C/s |

Figure 62:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 63:
Ordering Information

| Ordering Code | I ² C Bus | I ² C Address | Delivery Form | Delivery Quantity |
|---------------|----------------------|--------------------------|-------------------|-------------------|
| TMD37253 | 1.8V | 39h | Tape & Reel (13") | 5000 pcs/reel |

Buy our products or get free samples online at:

www.ams.com/ICdirect

Technical Support is available at:

www.ams.com/Technical-Support

Provide feedback about this document at:

www.ams.com/Document-Feedback

For further information and requests, e-mail us at:

ams_sales@ams.com

For sales offices, distributors and representatives, please visit:

www.ams.com/contact

Headquarters

ams AG
Tobelbader Strasse 30
8141 Premstaetten
Austria, Europe

Tel: +43 (0) 3136 500 0

Website: www.ams.com

RoHS Compliant & ams Green Statement

RoHS: The term RoHS compliant means that ams AG products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

ams Green (RoHS compliant and no Sb/Br): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

Important Information: The information provided in this statement represents ams AG knowledge and belief as of the date that it is provided. ams AG bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. ams AG has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ams AG and ams AG suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

Copyrights & Disclaimer

Copyright ams AG, Tobelbader Strasse 30, 8141 Premstaetten, Austria-Europe. Trademarks Registered. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

Devices sold by ams AG are covered by the warranty and patent indemnification provisions appearing in its General Terms of Trade. ams AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein. ams AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with ams AG for current information. This product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by ams AG for each application. This product is provided by ams AG "AS IS" and any express or implied warranties, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose are disclaimed.

ams AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of ams AG rendering of technical or other services.

Document Status

| Document Status | Product Status | Definition |
|--------------------------|-----------------|--|
| Product Preview | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice |
| Preliminary Datasheet | Pre-Production | Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice |
| Datasheet | Production | Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade |
| Datasheet (discontinued) | Discontinued | Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs |

Revision Information

| Changes from 0-02 (2016-May-19) to current revision 1-00 (2017-Mar-01) | Page |
|--|------|
| Completely revised version | |

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide

| | |
|-----------|--|
| 1 | General Description |
| 1 | Key Benefits & Features |
| 2 | Applications |
| 2 | Block Diagram |
| 3 | Pin Assignment |
| 4 | Absolute Maximum Ratings |
| 6 | Electrical Characteristics |
| 7 | Typical Operating Characteristics |
| 12 | Detailed Description |
| 12 | Proximity |
| 12 | Color and Ambient Light Sense |
| 12 | I ² C Characteristics |
| 13 | I ² C Write Transaction |
| 13 | I ² C Read Transaction |
| 13 | Timing Diagrams |
| 14 | Principles of Operation |
| 14 | System State Machine |
| 17 | Register Description |
| 17 | Register Overview |
| 19 | Detailed Register Description |
| 19 | Enable Register (Address 0x80) |
| 20 | ATIME Register (Address 0x81) |
| 20 | PTIME Register (Address 0x82) |
| 21 | WTIME Register (Address 0x83) |
| 21 | AILTL Register (Address 0x84) |
| 22 | AILTH Register (Address 0x85) |
| 22 | AIHTL Register (Address 0x86) |
| 23 | AIHTH Register (Address 0x87) |
| 23 | PILT Register (Address 0x88) |
| 24 | PIHT Register (Address 0x8A) |
| 24 | PERS Register (Address 0x8C) |
| 26 | CFG0 Register (Address 0x8D) |
| 27 | PCFG0 Register (Address 0x8E) |
| 28 | PCFG1 Register (Address 0x8F) |
| 29 | CFG1 Register (Address 0x90) |
| 29 | REVID Register (Address 0x91) |
| 30 | ID Register (Address 0x92) |
| 30 | Status Register (Address 0x93) |
| 31 | CDATAL Register (Address 0x94) |
| 31 | CDATAH Register (Address 0x95) |
| 31 | RDATAH Register (Address 0x96) |
| 31 | RDATAH Register (Address 0x97) |
| 32 | GDATAH Register (Address 0x98) |
| 32 | GDATAH Register (Address 0x99) |
| 32 | BDATAH Register (Address 0x9A) |
| 32 | BDATAH Register (Address 0x9B) |
| 33 | PDATA Register (Address 0x9C) |
| 33 | CFG2 Register (Address 0x9F) |
| 34 | CFG3 Register (Address 0xAB) |
| 35 | POFFSETL Register (Address 0xC0) |

| | |
|-----------|---|
| 35 | POFFSETH Register (Address 0xC1) |
| 36 | CALIB Register (Address 0xD7) |
| 37 | CALIBCFG Register (Address 0xD9) |
| 38 | CALIBSTAT Register (Address 0xDC) |
| 38 | INTENAB Register (Address 0xDD) |
| 39 | Application Information |
| 39 | Schematic |
| 40 | PCB Layout |
| 41 | Package Drawings & Markings |
| 43 | Tape & Reel Information |
| 44 | Soldering & Storage Information |
| 45 | Storage Information |
| 45 | Shelf Life |
| 45 | Floor Life |
| 45 | Rebaking Instructions |
| 46 | Ordering & Contact Information |
| 47 | RoHS Compliant & ams Green Statement |
| 48 | Copyrights & Disclaimer |
| 49 | Document Status |
| 50 | Revision Information |