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TSL2540 Daughter Card
ALS Device in FN package

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TSL2540 Daughter Card

Table of Contents

Sheet 1: Title Page

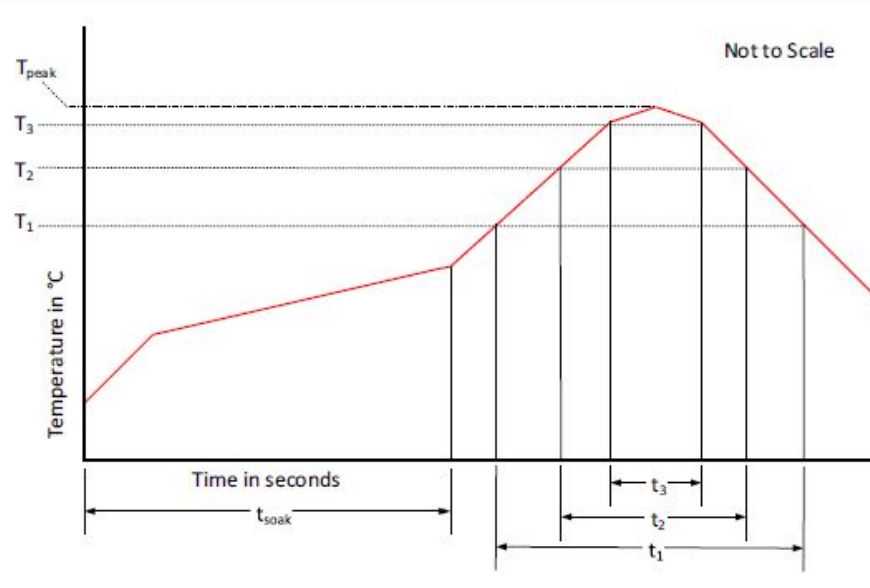
Sheet 2: Project Page (This page)

Sheet 3: Schematics

Revision History

Version: A C. Todd
Initial Release

Suggested Board Reflow Profile



Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/sec
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T_1)	t_1	Max 60 sec
Time above 230 °C (T_2)	t_2	Max 50 sec
Time above $T_{peak} - 10$ °C (T_3)	t_3	Max 10 sec
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max -5 °C/sec

Title: TSL2540 Daughter Card

Board Number: DC-TSL2540-01

Rev: A

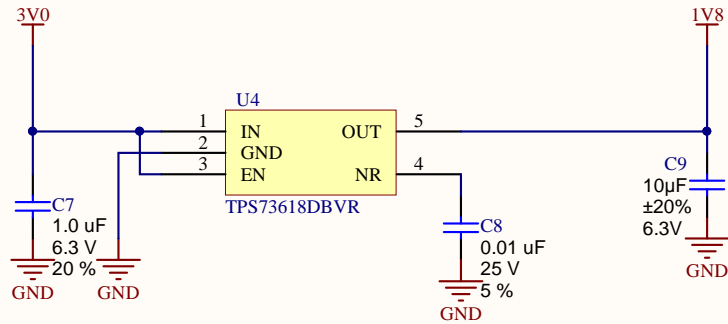


Date: 3/6/2017

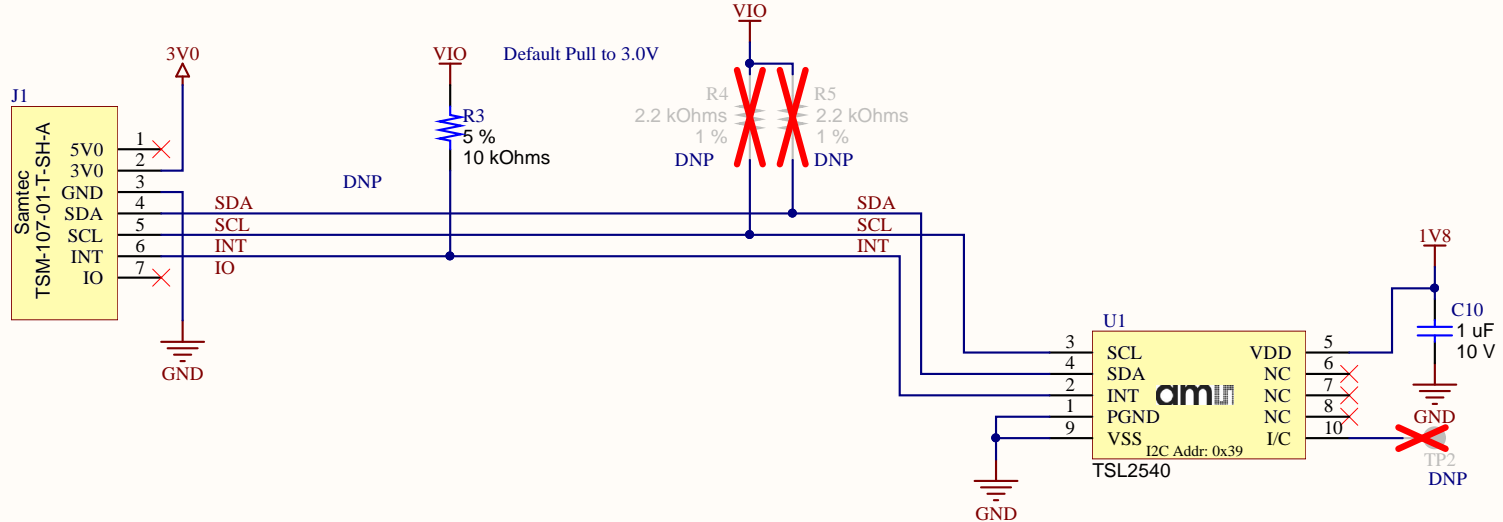
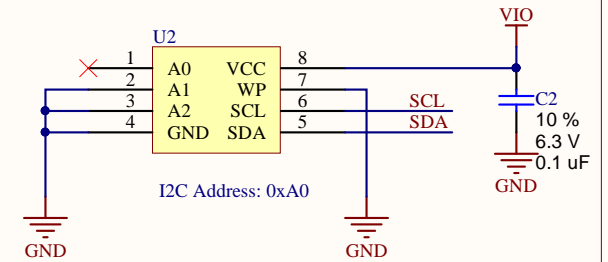
Author: C. Todd

Sheet 2 of 3

Regulator Bypass



EEPROM



Mounting Holes



Title: TSL2540 Daughter Card

Board Number: DC-TSL2540-01

Rev: A



Date: 3/6/2017

Author: C. Todd

Sheet 3 of 3

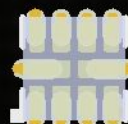
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DC-TSL2540-01

Rev: A

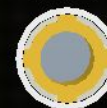
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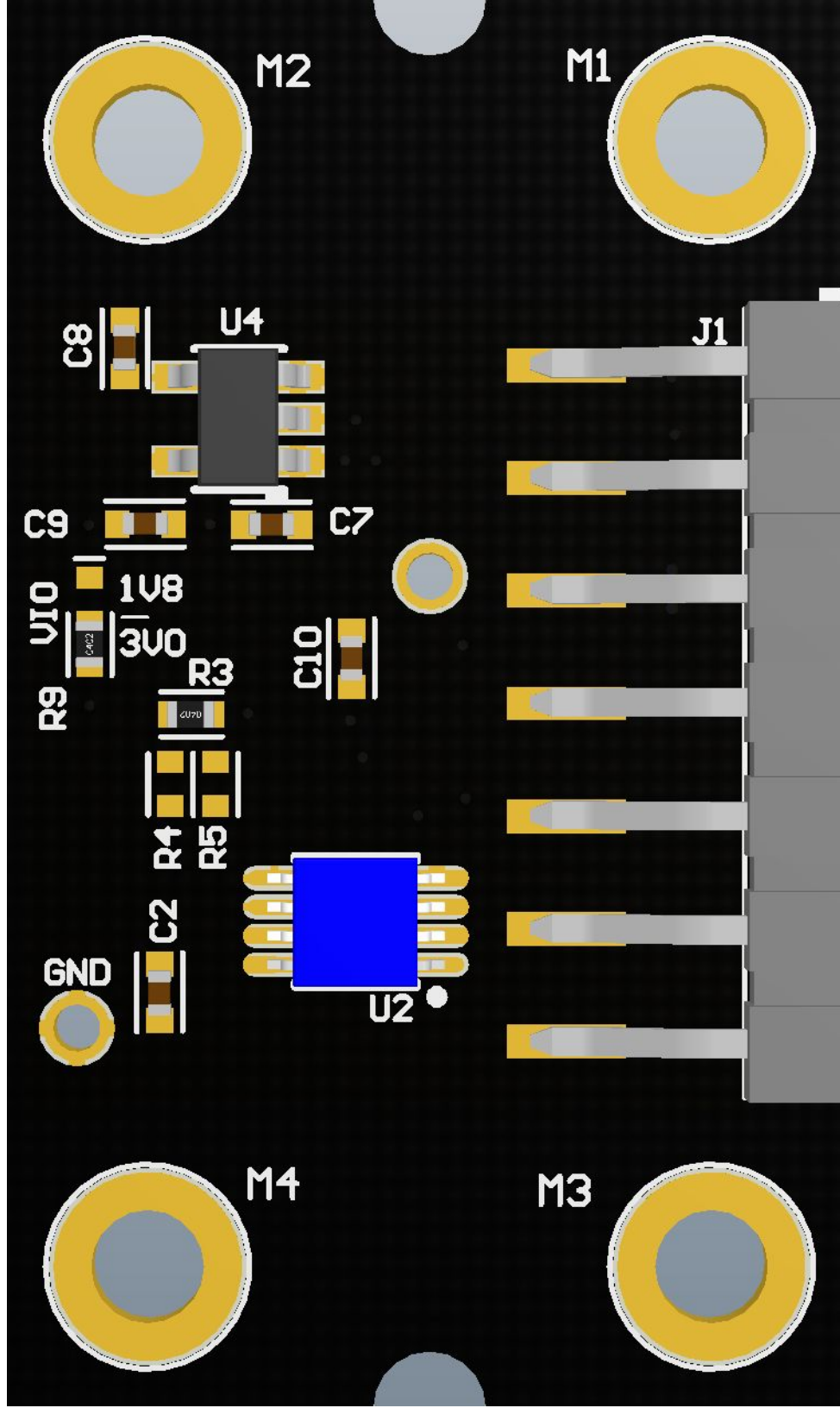
TP2
I/C

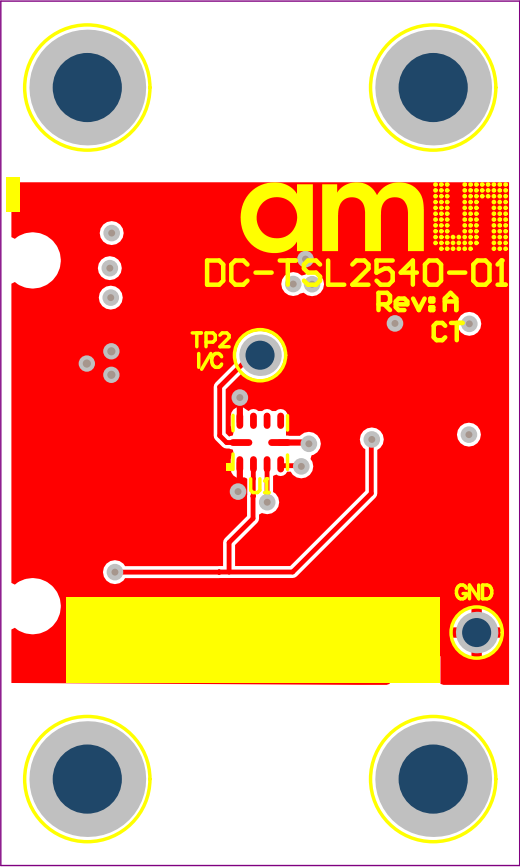


U1

GND







Board Details

- 1. Board Size: 750mil x 1250mil +/- 10%
- 2. Board Thickness: 62mil +/- 10%
- 3. Board material: FR4 with 0.5oz Copper
- 4. Component count: 20
- 5. Pad Count: 59
- 6. Hole Count: 29
- 7. Soldermask Color: Black
- 8. Silkscreen Color: White
- 9. No Silkscreen over exposed copper.
- 10. PCB Manufacturer not to add any additional silkscreen
- 11. Fabricate to IPC-600 Class 1 unless otherwise specified
- 12. RoHS compliant
- 13. Boards to be delivered with Tabs after Assembly

Layers Currently On

Title Block	
TOP	
Board Outline	Top Overlay
Multi-Layer	
Title TSL2540 Daughter Card	
Number DC-TSL2540-01	Rev A
Print Name Top Layer	
Variant: [No Variations]	Print Date: 3/6/2017
Drawn By: C. Todd	

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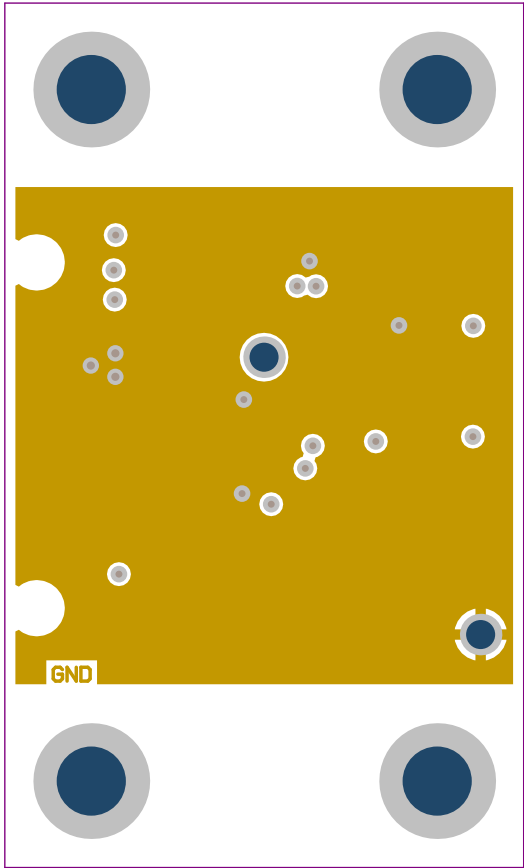
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Layers Currently On

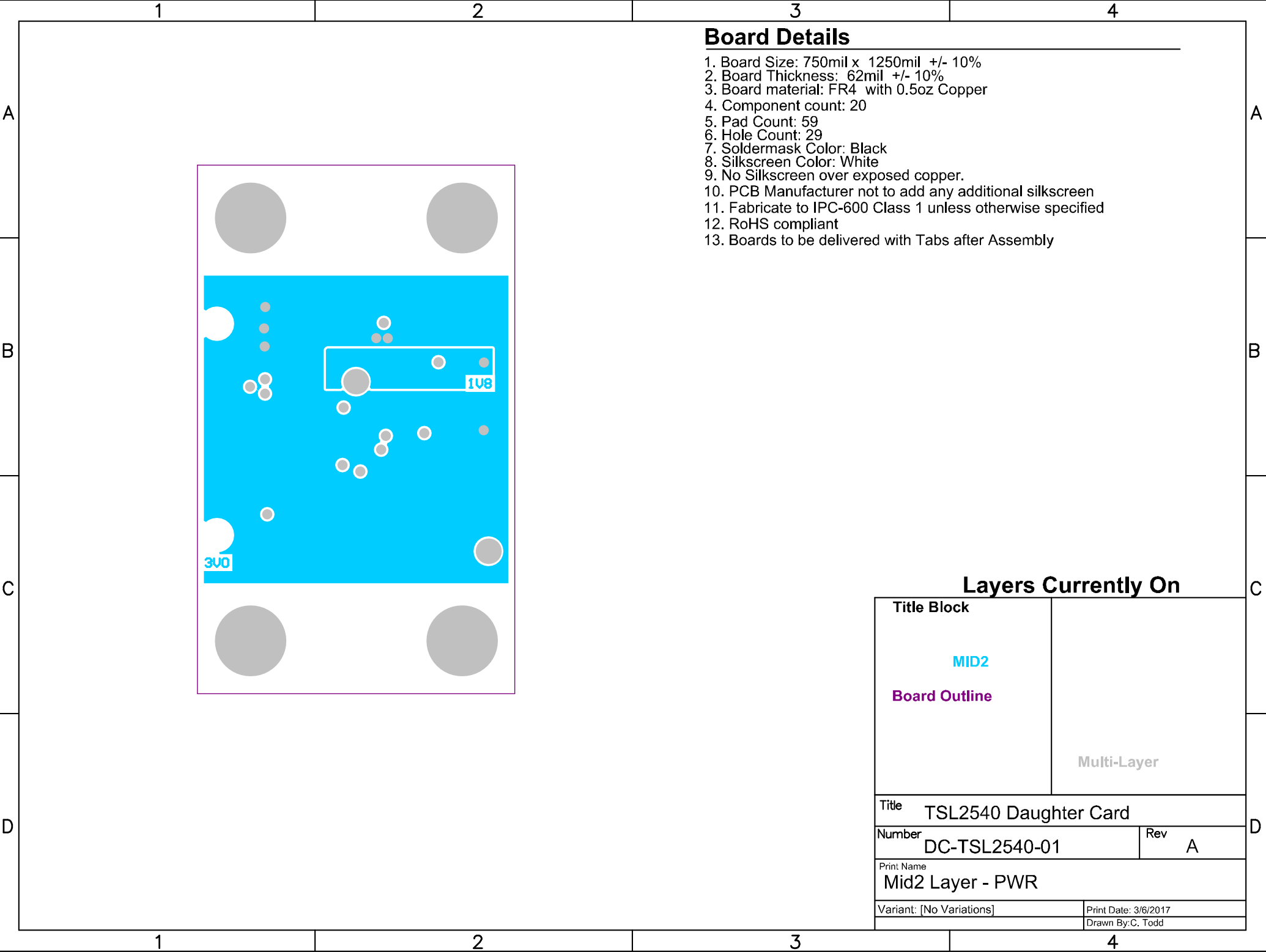
<div>Title Block</div> <div>MID1</div> <div>Board Outline</div>		<div>Multi-Layer</div>	
<div>Title</div> <div>TSL2540 Daughter Card</div>			
<div>Number</div> <div>DC-TSL2540-01</div>		<div>Rev</div> <div>A</div>	
<div>Print Name</div> <div>Mid1 Layer - GND</div>			
<div>Variant: [No Variations]</div>		<div>Print Date: 3/6/2017</div> <div>Drawn By: C. Todd</div>	

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Layers Currently On

Title Block			
MID2			
Board Outline		Multi-Layer	
Title TSL2540 Daughter Card			
Number DC-TSL2540-01		Rev A	
Print Name Mid2 Layer - PWR			
Variant: [No Variations]		Print Date: 3/6/2017	
		Drawn By: C. Todd	

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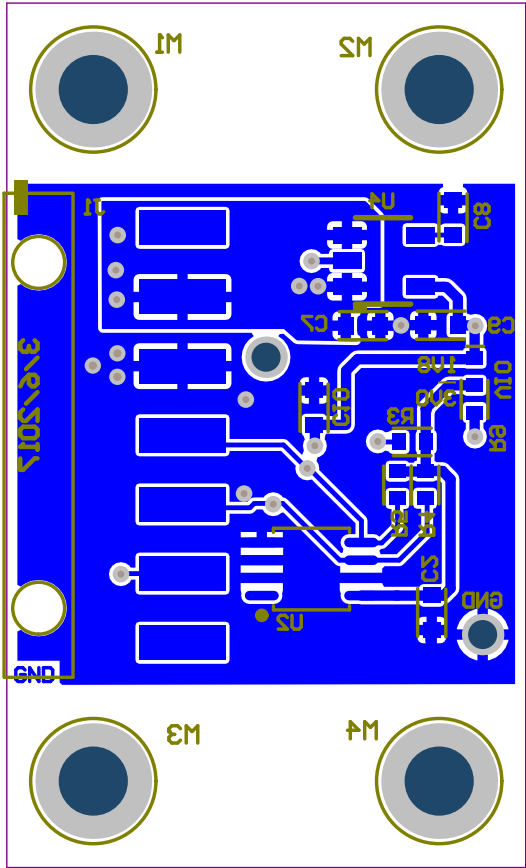
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Board Details

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Layers Currently On

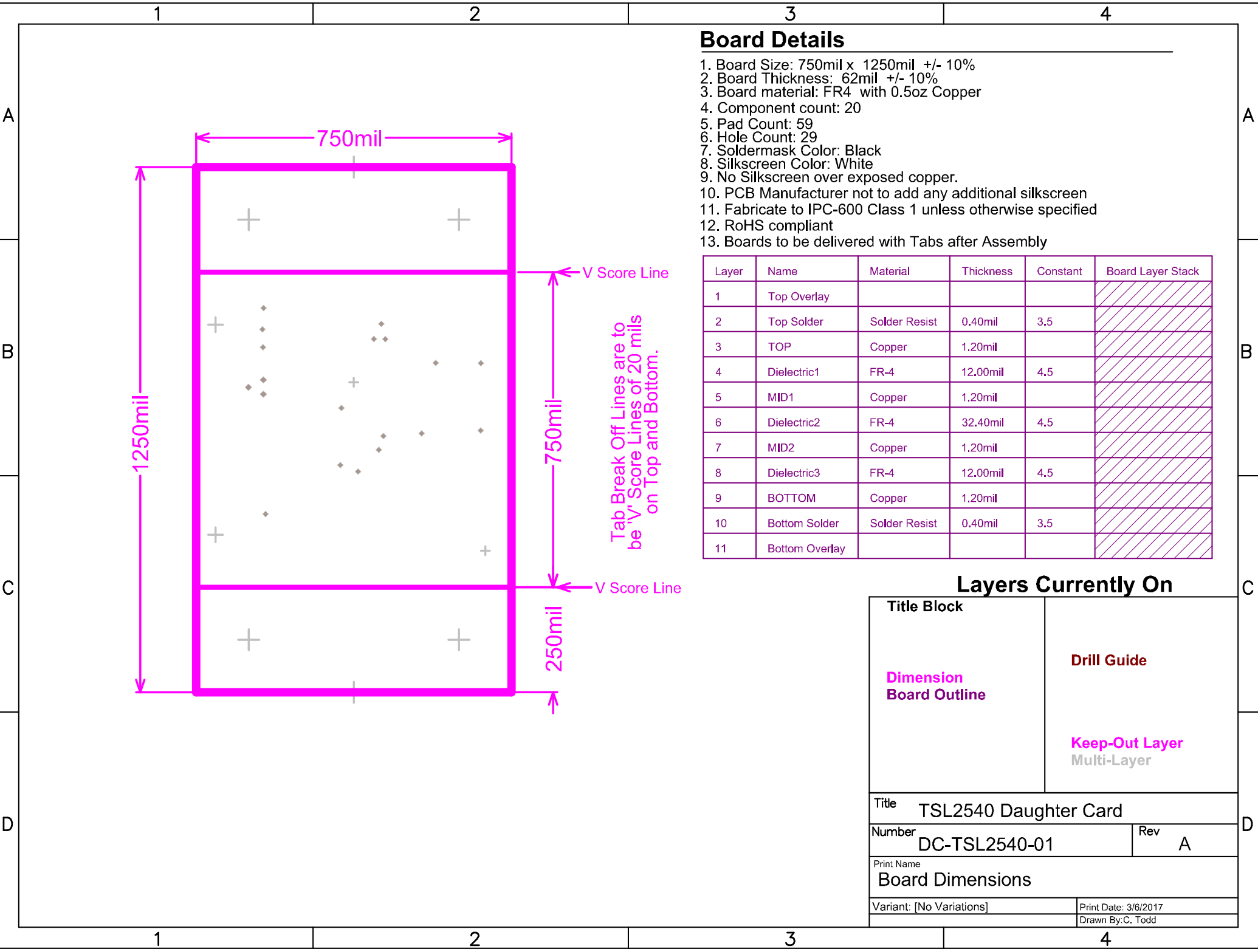
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BOTTOM		Bottom Overlay	
Board Outline		Multi-Layer	
Title TSL2540 Daughter Card			
Number DC-TSL2540-01		Rev A	
Print Name Bottom Layer			
Variant: [No Variations]		Print Date: 3/6/2017	
		Drawn By: C. Todd	

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Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				[Hatched]
2	Top Solder	Solder Resist	0.40mil	3.5	
3	TOP	Copper	1.20mil		[Hatched]
4	Dielectric1	FR-4	12.00mil	4.5	
5	MID1	Copper	1.20mil		[Hatched]
6	Dielectric2	FR-4	32.40mil	4.5	
7	MID2	Copper	1.20mil		[Hatched]
8	Dielectric3	FR-4	12.00mil	4.5	
9	BOTTOM	Copper	1.20mil		[Hatched]
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				[Hatched]

Layers Currently On

Title Block

Dimension Board Outline

Drill Guide

Keep-Out Layer Multi-Layer

TitleTSL2540 Daughter Card

NumberDC-TSL2540-01

RevA

Print NameBoard Dimensions

Variant: [No Variations]

Print Date: 3/6/2017

Drawn By: C. Todd

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A

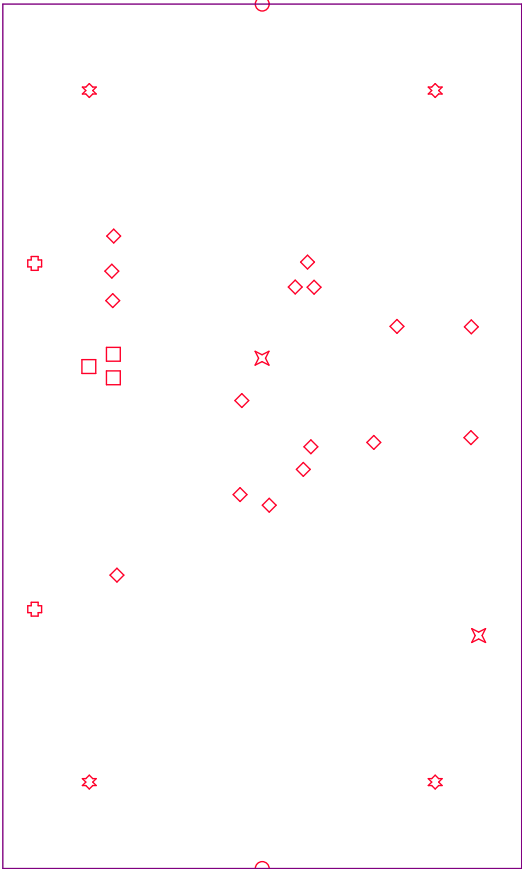
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Symbol	Count	Hole Size	Plated	Hole Type	Via/Pad	Pad Shape
⊗	2	42.00mil (1.067mm)	PTH	Round	Pad	Rounded
⊕	2	70.08mil (1.780mm)	NPTH	Round	Pad	Rounded
○	2	100.00mil (2.540mm)	NPTH	Round	Pad	Rectangle
□	3	11.81mil (0.300mm)	PTH	Round	Via	Rounded
☆	4	100.00mil (2.540mm)	PTH	Round	Pad	Rounded
◇	16	10.00mil (0.254mm)	PTH	Round	Via	Rounded
29 Total						

Layers Currently On

Title Block		Drill Drawing	
Board Outline			
Title TSL2540 Daughter Card			
Number DC-TSL2540-01		Rev A	
Print Name Drill Drawing			
Variant: [No Variations]		Print Date: 3/6/2017	
		Drawn By: C. Todd	

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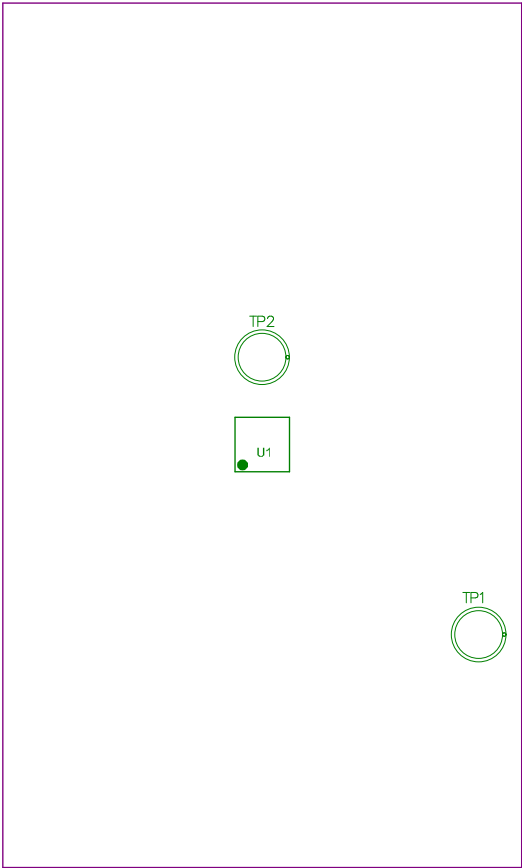
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Layers Currently On

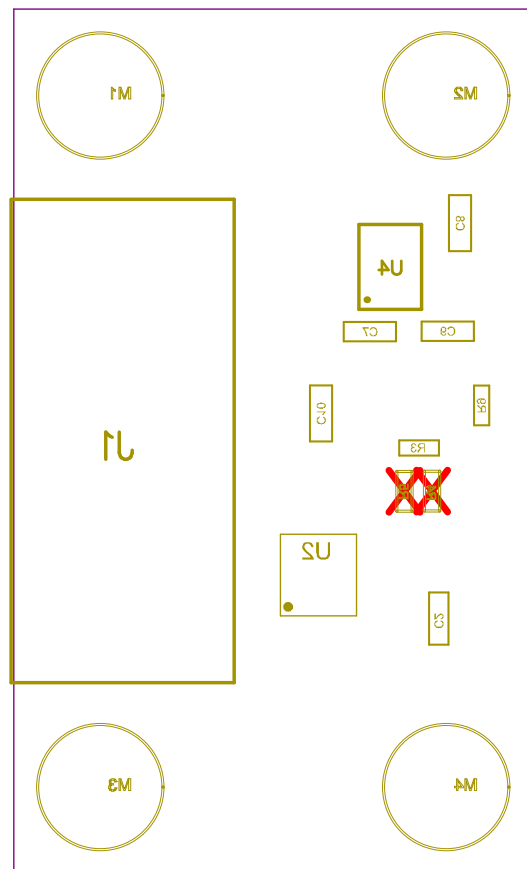
Title Block		Multi-Layer	
Board Outline Assembly Top			
Title TSL2540 Daughter Card			
Number DC-TSL2540-01		Rev A	
Print Name TOP Assembly			
Variant: Default Build		Print Date: 3/6/2017	
		Drawn By: C. Todd	

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8. Silkscreen Color: White
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10. PCB Manufacturer not to add any additional silkscreen
11. Fabricate to IPC-600 Class 1 unless otherwise specified
12. RoHS compliant
13. Boards to be delivered with Tabs after Assembly

Layers Currently On

<div> <div>Title Block</div> <div> <div>Board Outline</div> <div>Assembly Bottom</div> </div> <div>Multi-Layer</div> </div>	
<div>Title</div> <div>TSL2540 Daughter Card</div>	
<div>Number</div> <div>DC-TSL2540-01</div>	<div>Rev</div> <div>A</div>
<div>Print Name</div> <div>BOTTOM Assembly</div>	
<div>Variant: Default Build</div>	<div>Print Date: 3/6/2017</div>
<div>Drawn By: C. Todd</div>	

Bill of Materials

TSL2540 Daughter Card



Source Data From:	DC-TSL2540-01.PrjPcb
Project:	DC-TSL2540-01.PrjPcb
Variant:	Default Build

Creation Date	3/6/2017	4:06:25 PM
Print Date:	06-Mar-17	4:06:33 PM

Designator	Comment	Manufacturer	Manufacturer Part Number	Description	Quantity
C2	0.1uF,6V3, 0402, 10%	AVX	04026D104KAT4A	Cap 0.1uF,6V3, 0402, 10%	1
C7	1.0uF,6V3, 0402, 20%	AVX	04026D105MAT2A	Cap 1.0uF,6V3, 0402, 20%	1
C8	0.01uF,25V, 0402, 5%	Kemet	C0402C103J3RACTU	Cap 0.01uF,25V, 0402, 5%	1
C9	10uF,6V3,0402, 20%	Samsung Electro-Mechanics America, Inc	CL05A106MQ5NUNC	Cap 10uF,6V3, 0402, 20%	1
C10	1.0uF,10, 0402, 10%	Murata	GRM155R61A105KE15D	Cap 1.0uF,10v, 0402, 10%	1
J1	TSM-107-01-T-SH-A	Samtec	TSM-107-01-T-SH-A	Header, 7pin, Daughter Card SMT alignment	1
R3	10K,0402,5%	Vishay	CRCW040210K0JNED	Res, 10K, 0402, 5%	1
R9	0R	Vishay / Dale	CRCW04020000Z0ED	Res, 0R, 3 pin	1
U1	TSL2540	ams AG	TSL2540	TSL2540 - I2C Addr:0x39	1
U2	EEPROM Rohm BR24T04FVM-WTR	ROHM Semiconductor	BR24T04FVM-WTR	Serial EEPROM	1
U4	TPS73618DBVR	TI	TPS73618DBVR	1.8V Low Dropout Regulator	1
					11

Approved	Notes

Design Rules Verification Report

Filename : D:\SVN_Repo\Altium\Projects\DC-TSL2540-01\PCB.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=5mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Width Constraint (Min=5mil) (Max=100mil) (Preferred=7mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=15mil) (Conductor Width=6mil) (Air Gap=6mil) (Entries=4) (All)	0
Minimum Annular Ring (Minimum=5mil) (All)	0
Acute Angle Constraint (Minimum=30.000) (All)	0
Hole Size Constraint (Min=8mil) (Max=150mil) (All)	0
Hole To Hole Clearance (Gap=12mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=3mil) (All),(All)	0
Silk To Solder Mask (Clearance=2mil) (IsPad),(All)	0
Silk to Silk (Clearance=1mil) (Disabled)(All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Total	0

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for DC-TSL2540-01.PrjPcb

